Low-power and Small-area Transimpedance Amplifier with Active Inductor in 65 nm CMOS

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***Abstract*—This paper proposes a 25 Gbps, 0.67 pJ/bit inverter-based active-voltage current-feedback transimpedance amplifier (AVCF-TIA) circuit. The proposed TIA circuit has higher gain and wider bandwidth than the conventional AVCF-TIA circuit. In addition, the use of active inductors not only extends the bandwidth but also reduces the circuit area compared to the circuits using inductors. Post-layout simulation results show that the proposed TIA circuit has a transimpedance gain of 65.0 dBΩ and a bandwidth of 21.4 GHz. The proposed TIA circuit operates at a supply voltage of 1.0 V and consumes 16.8 mW (=16.8 mA×1.0 V). The area of the layout including I/O and DC pads is 670 μm × 580 μm (= 0.39 mm^2), and the area of the proposed TIA circuit is 185 μm × 170 μm (=0.031 mm^2).**

***Index Terms*—Transimpedance amplifier, Optical communication, TIA, AVCF, Low power consumption, Active inductor**

I. Introduction

In recent years, with the spread of communication devices such as smartphones and personal computers, the number of users has increased due to the diversification of information communication using these communication devices, such as SNS (Social Networking Service), video services, and online games. Hence, the amount of communication traffic is rapidly increasing. The increase in communication traffic has also led to a similarly rapid increase in power consumption at data centers [1]. Optical communication systems are a key technology supporting such high-speed communications, and the development of higher-performance optical communication systems is an important research issue in order to cope with increasing communication traffic in the future. The transimpedance amplifier (TIA) circuit is an integrated circuit used in the receiver system of high-speed optical communication systems. Therefore, TIA circuits are required to have high performance such as high gain and wide bandwidth, and many studies have been conducted [2]– [7].

In this paper, we propose an inverter-based TIA circuit that further improves the gain and extends the bandwidth by modifying an active voltage-current feedback TIA (AVCF-TIA) circuit. The proposed circuit consists of a TIA core circuit, two post-amplifier stages, and a 50 Ω buffer stage. The post-amplifier uses the active inductors to reduce circuit area and extend bandwidth. Post-layout simulations of the proposed inverter-based TIA circuit show that it has a transimpedance gain of 65.0 dBΩ, a bandwidth of 21.4 GHz, and a power consumption of 16.8 mW at 1.0 V supply voltage. The proposed TIA has a good eye aperture when a 25 Gbps PRBS signal was input at high amplitude.

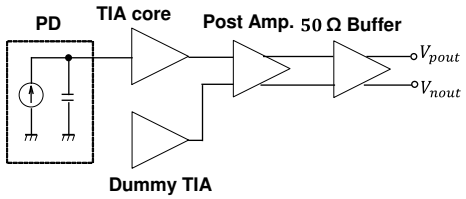

Fig. 1. The architecture of proposed TIA circuit.

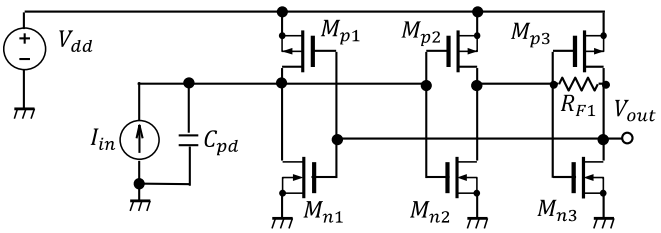

Fig. 2. The schematic of AVCF-TIA circuit.

II. Proposed TIA circuit

Figure 1 shows a schematic diagram of the proposed inverter-based TIA circuit. The proposed inverter-based TIA circuit consists of a TIA core circuit, a dummy TIA circuit, two post-amplifier stages, and a 50 Ω buffer. An active inductor is used in the post-amplifier 2 stage to extend the bandwidth. In the next subsection, the conventional AVCF-TIA circuit will be described, then the proposed inverter-based TIA circuit.

A. Conventional AVCF-TIA cirucuit

Figure 2 shows a conventional AVCF-TIA circuit. In the conventional circuit, output voltage V_{out} is applied to the gates of M_{n1} and M_{p1}, and input current I_{in} is applied to the drain; hence, the transimpedance gain is determined only by the transconductance g_{m1} of M_{n1} and M_{p1}, not by their resistances (Equation (1)). Therefore, the trade-off between transimpedance gain and bandwidth can be relaxed because transimpedance gain and bandwidth are no longer limited by each other. In addition, a two-stage inverter-based circuit consisting of M_{n2} and M_{p2}, M_{n3} and M_{p3} connected between

the input and output acts as a g_m-boosting amplifier, thereby reducing input impedance. The theoretical equations for the transimpedance gain, input impedance, damping factor, and natural frequency of the conventional AVCF-TIA circuit are as follows.

$$Z_T(0)_{conv} = \frac{1}{g_{m1}}, \tag{1}$$

$$Z_{in}(0)_{conv} = \frac{g_{m3}}{g_{m1}g_{m2}(g_{m3}R_{F1} - 1)}, \tag{2}$$

$$\xi_{conv} = \sqrt{\frac{C_{in}g_{m3}}{4C_{out}g_{m1}(g_{m2}R_{F1} - \frac{g_{m2}}{g_{m3}})}}, \tag{3}$$

$$\omega_{n,conv} = \sqrt{\frac{g_{m1}(g_{m2}g_{m3}R_{F1} - g_{m2})}{C_{in}C_{out}}}, \tag{4}$$

where the transconductance g_m is the sum of transistors M_n and M_p. The general solution for the bandwidth of a TIA circuit is expressed by

$$\omega_{-3dB} = \frac{1}{C_{in}Z_{in}}. \tag{5}$$

Therefore, the smaller the input impedance, the wider the bandwidth. The two-stage g_m-boosting amplifier has also the effect of increasing bandwidth because it reduces the input impedance. However, the conventional circuits have problems in achieving high gain and wide bandwidth operation. The conventional circuits have the advantage that the gain is determined by the transconductance only, but there is a limit to the value of the transconductance g_{m1}, which limits the gain, making it difficult to realize high-gain TIA circuits. In addition, there are concerns about an increase in power consumption due to an increase in the number of post-amplifiers caused by the gain limitation. The bandwidth is determined by the product of g_{m1}, which needs to be small to increase gain, and other element values need to be increased, but in addition to all element values being in the product, the small number of elements also makes bandwidth increase difficult. The following section shows the proposed inverter-based TIA circuit.

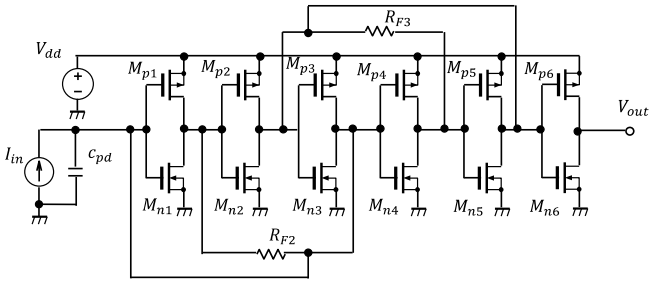

Fig. 3. Schematic of a proposed inverter-based TIA circuit.

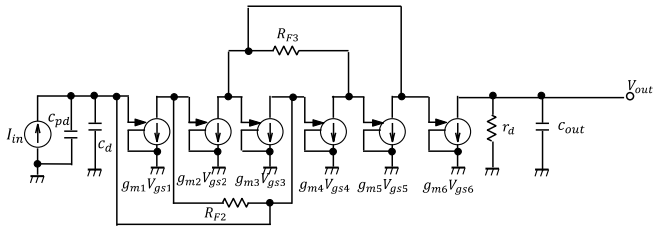

Fig. 4. Small-signal equivalent circuit of a proposed TIA.

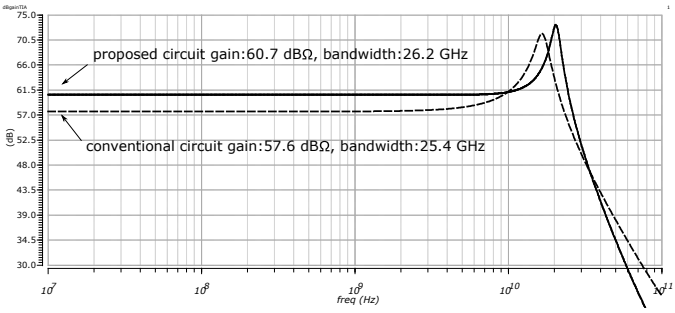

Fig. 5. A comparison of conventional and proposed TIA frequency responses.

B. proposed inverter-based TIA circuit

Figure 3 shows the proposed inverter-based TIA circuit. The inverter-based circuit consisting of M_{n1}–M_{n3} and M_{p1}–M_{p3} and the feedback resistor R_{F2} plays the same role as the conventional AVCF-TIA circuit because it has the same configuration as the conventional AVCF-TIA circuit. By adding M_{n4} and M_{p4}, M_{n5} and M_{p5} inverter-based circuits and feedback resistor R_{F3} in the next stage, the number of feedbacks is increased and the bandwidth is extended. The addition of an inverter-based circuit consisting of M_{n6} and M_{p6} is intended to improve the gain.

We will analyze the proposed inverter-based TIA circuit from the small-signal equivalent circuit and confirm its characteristics from theoretical equations. Figure 4 shows a small-signal equivalent circuit of the proposed inverter-based TIA circuit. Here, the g_{m1}–g_{m6} are the sum of the transconductances of the transistors M_n and M_p in each stage C_{pd}, C_d, and C_{out} are the parasitic capacitances of the PD and TIA circuits, and r_d is the internal resistance of the inverter-based circuit consisting of M_{n6} and M_{p6}. From the small-signal equivalent circuit, the transimpedance gain of the proposed circuit is

$$Z_T(0)_{prop} \approx -\frac{g_{m6}r_d}{g_{m3}}, \tag{6}$$

and it can be seen that the gain is increased by the added M_{n6} and M_{p6} inverter-based circuit. Also, the input impedance is

$$\begin{aligned} Z_{in}(0)_{prop} &= \frac{g_{m5}}{g_{m1}g_{m5} + X}, \\ X &= g_{m3}(g_{m2}(g_{m1}R_{F2} - 1) + g_{m4}(g_{m5}R_{F3} - 1)). \end{aligned} \tag{7}$$

From the aforementioned equation, we see that the addition of the inverter-based circuits of M_{n4} and M_{p4}, M_{n5} and M_{p5},

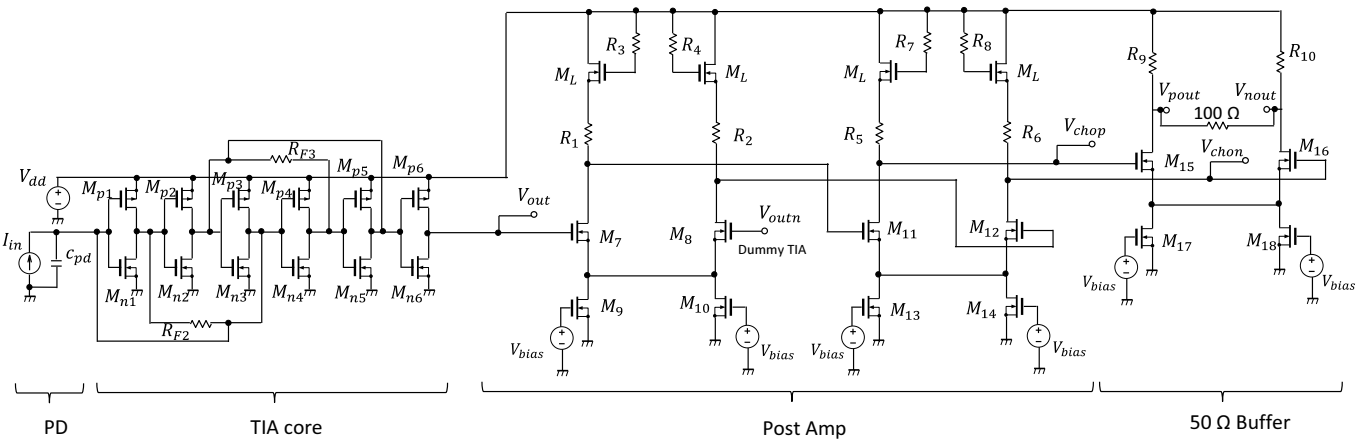

Fig. 6. Proposed TIA circuit schematic.

and the feedback resistor R_{F3} increases the product term as well as the term independent of g_{m3}, which is necessary to increase the transimpedance gain. Hence, the input impedance will be reduced and bandwidth will be expanded. The damping factor and natural frequency are as follows.

$$\xi_{prop} = \sqrt{\frac{(C_{out}r_d(g_{m1}g_{m5}+A)+C_{in}g_{m5})^2}{4C_{in}C_{out}r_d g_{m5}(g_{m1}g_{m5}+A)}}, \tag{8}$$

$$A = g_{m3}(g_{m2}(g_{m1}R_{F2}-1)+g_{m4}(g_{m5}R_{F3}-1)),$$

$$\omega_{n,prop} = \sqrt{\frac{g_{m1}g_{m5}+B}{C_{in}C_{out}r_d g_{m5}}}, \tag{9}$$

$$B = g_{m3}(g_{m2}(g_{m1}R_{F2}-1)+g_{m4}(g_{m5}R_{F3}-1)),$$

where $C_{in} = C_{pd} + C_d$. The increase in the number of elements has increased the damping factor term, which makes it easier to change the value of damping. It is also found that the damping can be significantly changed by changing the resistor R_{F3}.

C. Comparison of conventional circuit and proposed circuit

Figure 5 compares the pre-layout simulation results of the conventional circuit shown in Fig. 2 and the proposed circuit shown in Fig. 3. The results show that the gain of the proposed circuit is higher than that of the conventional circuit. In addition, -3 dB bandwidth shows that the proposed circuit has a slightly wider bandwidth. From these results, we see that the performance of the proposed circuit is better than that of the conventional circuit. The frequency response has a large peak, but this is not a problem because the peak was obtained by considering the simulation results after layout.

III. SCHEMATIC OF PROPOSED TIA CIRCUIT

Figure 6 shows the all TIA circuit including the proposed inverter-based TIA circuit. A current source and a 65 fF capacitor are connected at the input as an equivalent model of a PD. A dummy TIA circuit with the same schematic as the TIA core circuit is connected to one input of the first-stage post amplifier to provide differential signals. Two post-amplifiers

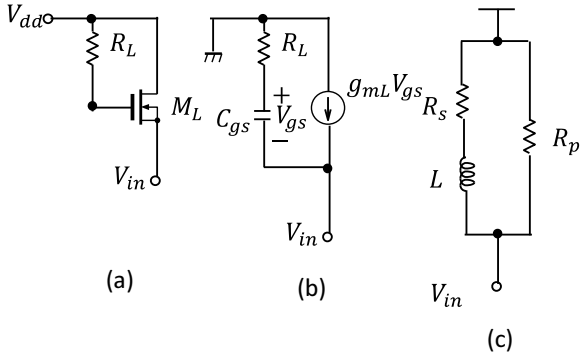

Fig. 7. (a) circuit schematic, (b)Small-signal equivalent circuit, (c) equivalent circuit of Wu folded active inductor.

are connected to the rear of the TIA core circuit, both of which have active inductors connected. In the final stage, a 50 Ω buffer circuit is connected for 50 Ω impedance matching. The all circuit was simulated by connecting 10 fF capacitances between gate–source, drain–GND, and source–GND to the active inductors, and connecting a 100 Ω resistor to the output of the 50 Ω buffer, considering the circuit connected in the subsequent stage.

A. active inductor

Figure 7(a) shows the circuit diagram of the active inductor used [8]. The reason for using active inductors is that a circuit configuration using spiral inductors requires a larger circuit area. Therefore, active inductors were used to extend the bandwidth while reducing the circuit area. Figure 7(b) shows the small-signal equivalent circuit of the active inductor. Here, C_{gs} is the internal capacitance of the transistor M_L. From this small-signal equivalent circuit, the input impedance is

$$Z_{in} = \frac{sC_{gs}R_L + 1}{sC_{gs} + g_{mL}}. \tag{10}$$

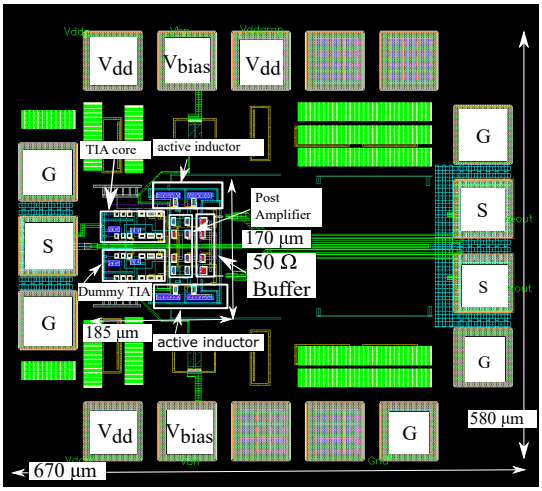

Fig. 8. post-layout simulation eyediagram of proposed TIA circuit.

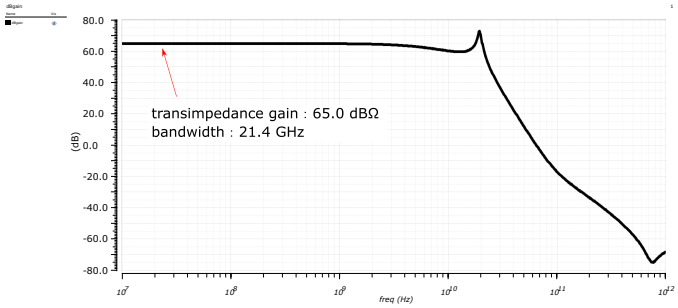

Fig. 9. post-layout simulation eyediagram of proposed TIA circuit.

Therefore, the input admittance is

$$Y_{in} = \frac{1}{Z_{in}} = \frac{1}{R_L} + \frac{1}{s\frac{R_L C_{gs}}{g_{mL}-\frac{1}{R_L}} + \frac{1}{g_{mL}-\frac{1}{R_L}}} = \frac{1}{R_p} + \frac{1}{sL+R_s}. \quad (11)$$

By changing the value of the resistor R_L, the effect of the inductance of the active inductor can be changed. From equation (11), the equivalent circuit of an active inductor can be drawn as shown in Fig. 7(c).

IV. Design of Proposed TIA Circuit Layout

A. LSI layout architecture

Figure 8 shows the layout of each circuit block and PAD layout. The layout consists of a TIA core circuit, a dummy TIA circuit, two post-amplifier stages, and a 50 Ω buffer. The area of the layout including I/O and DC pads is 670 μm × 580 μm (=0.39 mm^2), and the area of the proposed TIA circuit is 185 μm × 170 μm (=0.031 mm^2).

B. Result of post-layout simulation

Figure 9 shows the post-layout simulation results of the proposed TIA circuit. Post-layout simulations resulted in a transimpedance gain of 65.0 dBΩ and a bandwidth of 21.4 GHz in the Chebyshev approximation. The power consumption was 16.8 mW (=16.8 mA×1.0 mV). Figure 10 depicts the eye diagram for PRBS 7 with an input signal of 1.6 $\mathrm{mA_{pp}}$, 25 Gbps, and 20 ps rise and fall time. The differential output amplitude is 474 $\mathrm{mV_{ppd}}$, the eye opening width is 303 $\mathrm{mV_{ppd}}$, and the open degree is 64 %, thus obtaining a good eye opening.

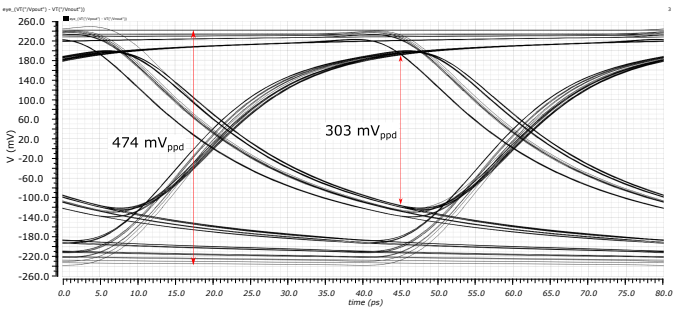

Fig. 10. post-layout simulation eyediagram of proposed TIA circuit.

C. comparison of post-layout simulation results

Table 1 summarizes a comparison of the proposed TIA circuit and the TIA circuits in previous papers. The evaluation index (FoM) is calculated by the following equation.

$$\mathrm{FoM} = \frac{\mathrm{Transimpedance}(\Omega) \times \mathrm{Bandwidth}(\mathrm{THz})}{\mathrm{Area}(\mathrm{mm}^2) \times \mathrm{Power}(\mathrm{mW})}. \quad (12)$$

From this table, we show that the proposed circuit has a very small circuit area and low power consumption, resulting in a higher FoM value than other circuits.

V. Conclusion

In this paper, the entire TIA circuit including the TIA core circuit is designed and simulated in 65 nm CMOS technology by modifying the conventional AVCF-TIA circuit. Post-layout simulation results show that the proposed circuit has a transimpedance gain of 65.0 dBΩ and a bandwidth of 21.4 GHz. The power consumption is as low as 16.8 mW and the power efficiency is 0.67 pJ/bit at 25 Gbps. Therefore, the proposed circuit is a low area and low power TIA circuit that can operate at 25 Gbps.

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References

[1] K. Saegusa, *Impact of Progress of Information Society on Energy Consumption (Vol. 2): Current Status and Future Forecast of Data Center Energy Consumption and Technical Issues*, Japan Science and Technology Agency (JST), 2021.

[2] G. Zhou, *et al.*, "A 30 Gbps 1.25 pJ/b CMOS receiver analog front-end with low supply voltage," *IEICE Electronics Express*, vol. 18 no. 8, 20210114, 2021.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER TIAS WORKS.

Reference (Year)	[3] (2014)	[4] (2014)	[5] (2018)	[2] (2021)	[6] (2023)	**This work (2024)**
CMOS Technology (nm)	65	65	65	40	65	65
Supply voltage (V)	3.3/1.0	1.2	1.0	1.0	1.2	1.0
TIA topology	RGC	RGC	RGC	Inv. +AVCF	Inv. +AVCF	Inverter
Trans-impedance gain (dBΩ)	76.9	52.0	65.8	63.8	70.7	65.0
Bandwidth (GHz)	21.4	50	11.0	24.3	16.3	21.4
Data rate (Gb/s)	28	52	–	30	25	25 **
Occupied area (mm^2)	0.32	0.48	0.25	0.63	0.39 (0.093) *	0.39 (0.031) *
Total power consumption (mW)	137.5	49.2	66	37.5	22.6	16.8
Energy efficiency (pJ/bit)	4.9	0.94	–	1.25	0.90	0.67
FoM ($\Omega\cdot THz/mm^2\cdot mW$)	3.40	0.84	1.30	1.60	6.34 (26.6) *	5.81 (73.1) *

*: Active area only, **: input current with high amplitude.

[3] T. Takemoto, *et al*., "A 25-Gb/s 2.2-W 65-nm CMOS optical transceiver using a power-supply-variation-tolerant analog front end and data-format conversion," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 471–485, Feb. 2014.

[4] S.G. Kim, *et al*., "A 50-Gb/s differential transimpedance amplifier in 65nm CMOS technology," in Proc. 2014 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2014, pp. 357–360.

[5] R. Costanzo, *et al*.,"A current reuse regulated cascode CMOS transimpedance amplifier with 11-GHz bandwidth," *IEEE Microw. Wirel. Compon. Lett.*, vol. 28, no. 9, pp. 816–818, Sept. 2018.

[6] K. Tominaga, and Y. Takahashi, "Low-power, 25-Gbps Active Voltage Current Feedback Transimpedance Amplifier in 65-nm CMOS," in Proc. IEEE Int. Conf. Electro., Info., and Commu. (ICEIC), Taipei Taiwan, Ju. 28–31, 2024, pp. 120–123.

[7] A. Tsuchiya, *et al*., "Design of a 45 Gb/s, 98 fJ/bit, 0.02 mm^2 transimpedance amplifier with peaking-dedicated inductor in 65-nm CMOS," IEICE Trans. Electronics, vol. E103-C no. 10, pp. 489–49, Oct. 2020.

[8] F. Yuan, *CMOS Active Inductors and Transformers Principle, Implementation, and Applications*, Springer Science+Business Media, LLC, 2008.