## A 11pA/√Hz TIA with +15dB input OMA range for 112Gb/s PAM4 Optical Links in 22nm FDSOI

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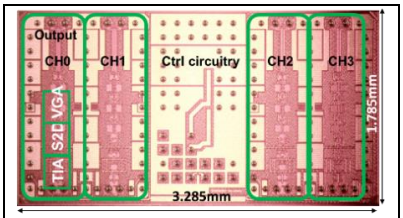
High-speed optical links are advancing towards higher density and bandwidth (BW) to facilitate the scaling of data centers. A transimpedance amplifier (TIA) is a critical component in the optical chain that significantly affects the noise, BW, linearity, and power consumption of intensity modulated optical links. Recently, CMOS inverter-based shunt-feedback (IBSF) TIAs (Fig. 1) have proven satisfactory noise and BW performance for 100Gb/s receivers [1-4]. However, they do so by trading off linear dynamic range. The use of large feedback resistor ($R_f$) to improve noise, compromises the linearity of the TIA at high input currents. Furthermore, most IBSF-TIAs operate from an effective 1V supply voltage [1-4], exacerbating this tradeoff. Nevertheless, based on IEEE specifications, it is imperative to meet bit-error-rate (BER) of 4.8E-4 with margin up to +4dBm of optical modulation amplitude (OMA). This corresponds to photodiode (PD) currents of 2.5mApp for a responsivity of 0.8 A/W. To understand the trade-off, Fig. 1 plots the signal-to-noise-and-distortion ratio (SNDR) for three different TIA designs. Each design is optimized for a different $R_f$ value, and includes the full amplifier chain. At low OMA inputs, TIA is noise limited; hence the TIA with larger $R_f$ provides the best SNDR in that region. However, at high OMA input, where the performance is linearity limited, the TIA using smallest $R_f$ provides better SNDR. Nevertheless, none of the TIAs satisfy the required specifications between -6dBm to +4dBm. To extend the dynamic range, one could adjust the $R_f$ dynamically inside the automatic gain control (AGC) loop [5], however this approach only modulates the low frequency part of the transimpedance ($Z_t$) and causes irreparable damage to the quality of the PAM4 eye. Alternatively, a variable optical attenuator (VOA) can be employed in the optical receiver to reduce the maximum input current. This comes at the expense of larger power consumption and/or more complexity in the AGC loop. In this work, a CMOS TIA is proposed to overcome the linearity-noise trade-off in IBSF TIAs.

Fig. 2 demonstrates the block diagram and the detailed circuit diagram of the proposed TIA. A SF CMOS inverter forms the TIA stage. An inductive peaking network inside the feedback loop [6] extends the BW while improving the noise performance of the TIA. A push-pull source follower (PPSF) circuit buffers the TIA output to both the inverting unity gain (IUG) stage and the VGA. The PPSF reduces loading on the TIA and eliminates extensive peaking in that node; hence improving the group delay (GD) variation of the TIA. The IUG stage for creating inverted signal is composed of $g_m \times 1/g_m$ inverters [1]. Two series peaking inductors are designed to align the high frequency response of the positive and negative outputs. A low frequency feedback senses the DC common-mode (CM) voltages of single-ended to differential (S2D) converter and adjusts the NMOS source-follower gate voltages to balance them. This is a critical loop to align the CM voltages across process corners and temperature variations. Once the signal is differential**,** a VGA along with gain stages provide the required dynamic range of the TIA. Two LDOs operating from 1.8V provide the required voltage for the TIA (1V) and VGAs (1.7V) while rejecting the supply noise.

Fig. 3 highlights the block diagram and the detailed schematic of the overload mitigation circuitry (OMC). It is composed of a switch connected to the input network of the TIA operating as a variable resistor and an inverter with a resistive SF akin to the main TIA. The central idea is to redirect the RF current coming into the TIA to the dummy TIA at overload condition without impacting the phase response. The dummy TIA acts as a low impedance path with the same CM voltage for the current and should be sized depending on the required attenuation and main TIA impedance. As shown in Fig. 3, the switch is controlled through the AGC loop and is slowly activated before the TIA stage saturates. Hence, at maximum gain when the performance is noise limited the switch is OFF with no attenuation and a negligible noise contribution due to capacitive loading at the TIA input. Then, it gradually turns ON before the TIA saturates and it is fully active at minimum gain where the receiver performance is distortion limited. In this design, the OMC can drop the $Z_t$ by 7dB at the expense of 6mW extra power consumption. Using this technique, the performance of the TIA can be extended over the input OMA range of -10 to +5dBm. The simulated noise and total harmonic distortion (THD) performance of the TIA in AGC mode versus input OMA is also highlighted in Fig. 3 for three different cases: 1) The OMC is fully OFF, 2) The OMC is fully ON & 3) The OMC is OFF at high gains and turns on slowly before the TIA saturates. As can be seen, case 1 shows the best noise performance while case 2 shows the best linearity performance, however, case 3 demonstrates the best noise performance at high gain and best linearity performance at low gain. This leads to a large input dynamic range while burning low power consumption at the dummy TIA stage.



Die micrograph.

The die photo of 4 channel TIA fabricated in 22nm-FDSOI CMOS technology is shown in the micrograph photo. Fig. 4 highlights the measured and simulated S21 (single-ended input to differential output) and S11 of the TIA at minimum and maximum gain. S11 changes due to OMC operation. Using the measured S-parameters and the PD model, the transimpedance response of the TIA across gain control is plotted in Fig. 4. The TIA achieves more than 32dB of dynamic range with small variation in the magnitude response through VGA control. The GD of the TIA at maximum gain is also shown in Fig. 4. It varies less than 6ps up to Nyquist frequency.

The optical characterization setup is shown in Fig. 5. Here we leverage an in-house transmitter comprised of a silicon-photonic (SiPh) Mach-Zehnder modulator and a custom PAM4 driver. To minimize crosstalk, parasitic inductance, and capacitance, the TIA is flip chip mounted on a SiPh receiver-IC containing the PD. A copper heatsink is added to the Stacked Die Assembly (SDA) to emulate production assembly. A commercially available, third-party PAM4 DSP chip running at 56GSa/s provides digital equalization, digital to analog conversion in TX, analog-to-digital conversion in RX, and total link BER measurement. PRBS15 is mapped to PAM4 for the characterization. The BER versus input OMA is also highlighted in Fig. 5. The red curve illustrates the performance of the TIA where it meets the IEEE specification for more than 15dB input OMA. Green curve demonstrates the case where the OMC is OFF. The TIA sensitivity is as good as the red curve; however, the distortion degrades the performance starting at OMA of 0dBm. The blue curve is measured when the OMC is fully ON which leads to degraded sensitivity at low OMA input levels and excellent linearity at high input OMA. This plot clearly shows that this design is optimized to provide the best sensitivity and linearity performance at minimum and maximum input OMAs, respectively. Figure 6 shows the performance summary and comparison with the state-of-the-art TIAs indicating competitive noise performance while achieving operation over +15dB of input OMA with only 155mW per channel of power consumption. Although the power consumption is higher than the other works shown in table, they all require VOA in the optical receiver to meet the BER specification at high OMAs. This adds significant power (for thermal VOAs) or complexity (for MZM based VOA) penalty to the chain. To the best of the authors' knowledge, this is the first IBSF TIA that covers the whole 100Gb/s PAM4 OMA with effective 1V supply voltage at the input stage.

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**References:**

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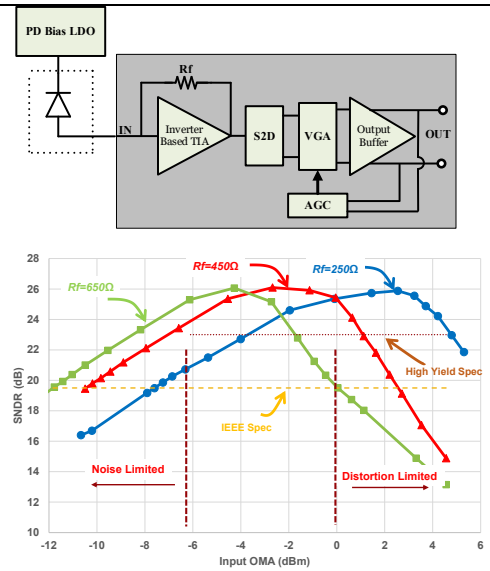


Fig. 1 Block diagram of a single-ended IBSF CMOS TIA and SNDR performance of the TIA chain designed for 3 different SF resistor values.

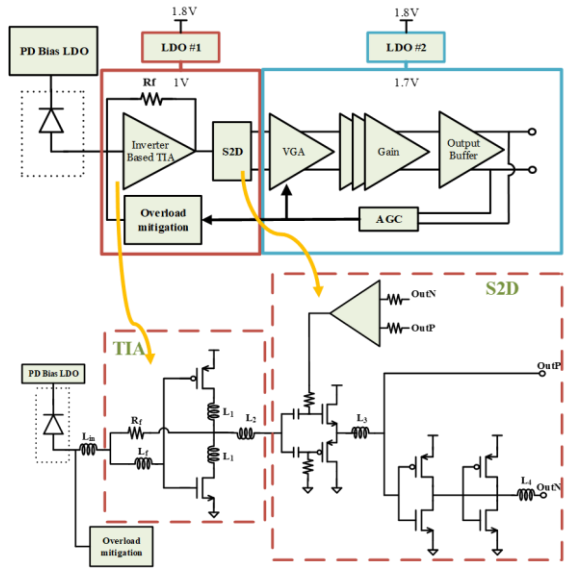


Fig. 2. Block diagram of the proposed TIA and detailed schematic of the TIA stage and S2D block.

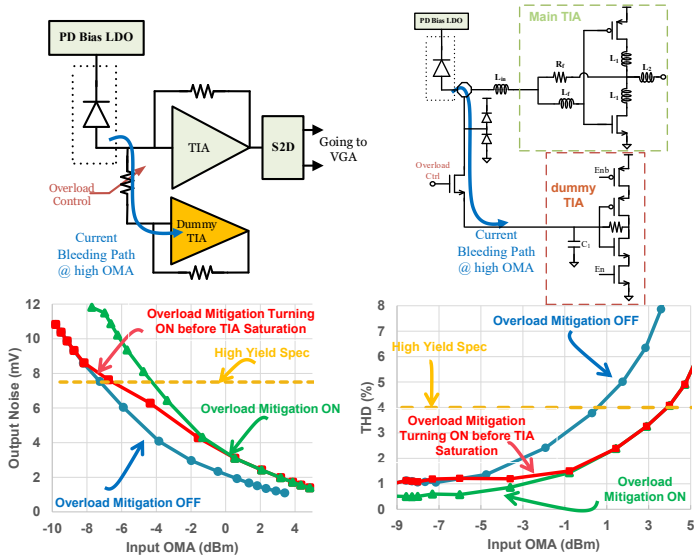


Fig. 3. Block diagram and schematic of proposed OMC technique, output noise and THD performance at different OMC states.

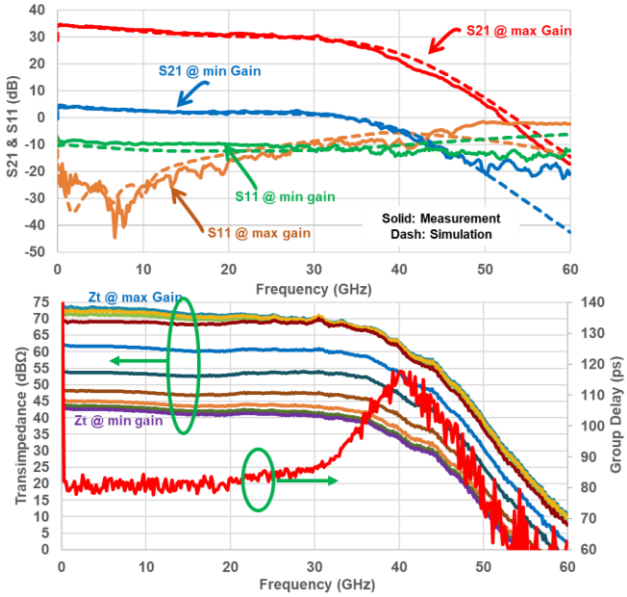


Fig. 4. Measured and simulated S21 & S11, $Z_t$ and GD of the TIA.

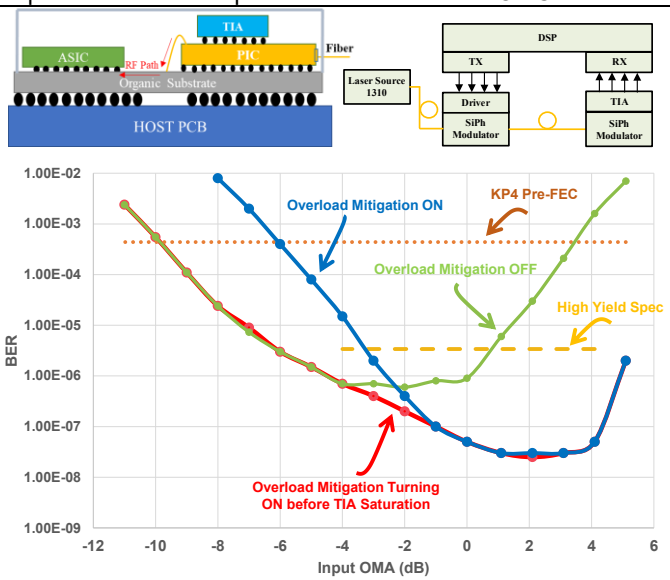


Fig. 5. SDA of the TIA and photodiodes and optical test setup. BER performance of the TIA for different OMC states.

| Parameter | | This work | ISSCC 23 [2] | JSSC'19 [1] | JSSC '22 [3] |
|---|---|---|---|---|---|
| Technology | | 22nm FD-SOI | 16nm FinFET | 16nm FinFET | 28nm Bulk |
| Data Rate (Gb/s) | | 106.25 | 106.25 | 106.5 | 100 |
| Max $Zt$ | | 74 dBΩ | 75.5 dBΩ | 78 | 68 |
| Min $Zt$ | | 47 dBΩ | NA | NA | NA |
| Input Referred Noise | | 11 pA/√Hz | 7 pA/√Hz | 16.7pA/√Hz | 17pA/√Hz |
| Output Swing | | 550mV | 600mV | 300mV[1] | 600mV[1] |
| $BW_{3dB}$ | @ Max $Z_t$ | 28 GHz | 18.4 GHz | 27GHz | 20GHz |
| | @ Min $Z_t$ | 34GHz | NA | NA | NA |
| THD (%) | @ Max $Z_t$ | <2.5 | <2.5 | <2.5 | NA |
| | @ Min $Z_t$ | <4 | NA | NA | NA |
| Sensitivity @ KP4 pre-FEC SER (dBm) | @ Min OMA | -10 | -13.97 | -11 | -8.9 |
| | @ Max OMA | >+5 | NA | NA | NA |
| Power per Channel (mW) | | 155 | 108 | 60.8 | 117 |

[1]without 50Ω termination

Fig. 6 Performance summary and comparison with state-of-the-art works in literature.