A 44μW 140dB-DR Hybrid Light-to-Digital Converter with Current-Tracking Dynamic Zoom and Power-Scaling OTA

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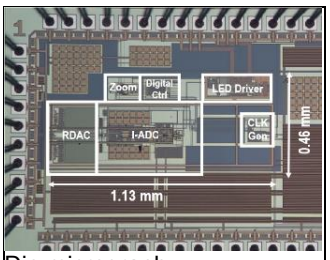
Highly sensitive optical sensors have been widely used in chemical analysis, backlight control, gas detection, and medical devices. For instance, photoplethysmography (PPG) sensors can assess one's heart rate, oxygen saturation (SpO_2), and pulse wave velocity. These applications often require light-to-digital converters (LDCs) with large dynamic range (DR) in excess of 120dB to sense currents from a few pA to hundreds of μA. State-of-the-art LDCs that operate in the time or frequency domain, such as slope ADCs [1-2] and Hourglass ADCs [3], achieve excellent DR by employing auxiliary DC servo loop [1-2] or predictive DAC [3] to cancel the baseline input current before the ΔΣ conversion. However, these auxiliary feedback loops have limited bandwidth (BW), and therefore their slow response cannot track fast-changing current disturbances. Continuous-time ΔΣ modulators (CT-ΔΣM) based on an incremental transimpedance amplifier (TIA) [4] or a truncation baseline-servo loop [5] achieve over 136dB DR in kHz BW. However, the former dissipates >1mW due to the power-hungry loop filter and segmented DAC, while the latter is not compatible with time-multiplexed input for two-wavelength SpO_2 or linear pixel array.

This paper proposes an alternative hybrid incremental ΔΣM (I-ΔΣM) that works for time-multiplexed input currents. This I-ΔΣM combines current-mode static zoom (SZ) and dynamic zoom (DZ) to achieve 140dB DR while being able to cope with significant DC and AC input currents up to 230μA. The power-efficient SZ and DZ, together with a power-scaling loop integrator, significantly reduce the power of the I-ΔΣM to 44μW, leading to a best-in-class FoM_S of 216.5dB.

In Fig.1, the LDC employs a 2nd-order I-ΔΣM with hybrid CT-DT loop filters. In addition, the 8b-SZ and 1b-DZ loops digitize the baseline and the fast-varying input currents, respectively. Their outputs are accumulated in digital domain and then drive an 8b resistive DAC (RDAC), which provide up to 230μA compensation current to prevent the core I-ΔΣM from being saturated. The residual input current is fine converted by the I-ΔΣM. To optimize the dynamic power, the first integrator utilizes OTA slicing technique where the number of active OTAs is reduced with the conversion cycle. This exploits the fact that the noise weight of the I-ΔΣM also decreases with clock cycles [6]. Fig.1 (right bottom) illustrates the simplified timing diagram of a two-wavelength SpO_2 test. When the LED is off, SZ is enabled to detect ambient light (AMB). Once the LED is on, SZ is repeated to measure ambient light plus baseline signal (AMB+DC). Both components are fed back and subtracted from the input signal, leaving only the AC component as the net input current to the I-ΔΣM. Following SZ, DZ is engaged during I-ΔΣM conversion to detect and compensate large AC input currents exceeding the I-ΔΣM input range. Furthermore, the 8b output of SZ is filtered and used to adjust the LED current over a range of 0-61 mA. This ensures optimal system signal-to-noise ratio (SNR) when light strikes the receiver from different distances.

Ambient light and baseline input signals severely curtail the input DR of conventional ΔΣMs and therefore reduce their power efficiency [4]. In this work, large DC input currents are calibrated by SZ in a power efficient manner. Fig.2 (top) shows the SZ implemented by a RDAC and a synchronous 8b SAR ADC. During the SZ period, the slicing OTA is configured as a TIA to convert the I_{PD} into an output voltage. The SAR ADC identifies the polarity and magnitude of I_{PD} in 8 cycles and reconfigures the RDAC to generate compensation current such that the residual current I_{AC} is limited to less than ±2μA. Furthermore, since only the residual AC input current is integrated, the integration capacitor has been reduced to 20pF, a 5× reduction compared to [1].

OTA slicing is enabled during I-ΔΣ conversion to save power. In Fig.2 (bottom left), two OTA slices are replicated at a ratio of 1:3, and each slice contains two cascaded current-reuse G_m cells. The OTA slicing technique explores the fact that the decimation of I-ΔΣM causes non-uniform weighting of I_{AC} and the associated noise contribution of the OTA, such that OTA power can be reduced by introducing affordable noise penalty. Fig.2 (bottom right) shows the simulated input-referred noise (IRN) $V_{n,in}$ and averaged OTA power versus a conversion cycle k, at which slice 2 is disabled. The later slice 2 is off, the less obvious the IRN reduction is, while the opposite is true for the OTA power. In this work, slice 2 is powered off in the last 350 cycles, resulting in a slight increase of IRN to $2\mu V_{rms}$ but a nearly 2× decrease in OTA power from 63μW to 35μW.



Die micrograph.

Rapidly rising interference currents, caused by artificial lighting, motion artifacts, and light on/off moments, have large magnitude and thus can saturate the I-ΔΣM. We propose a DZ technique to achieve on-the-fly tracking and compensation of the fast-varying, large-amplitude input currents during I-ΔΣM conversion. As shown in Fig.3 (top), the basic principle of DZ is to estimate the I_{AC} by examining V_{O1} during a fixed integration interval Δt. When I_{AC} exceeds the preset threshold range of ±1μA, the DZ loop steers a compensation current to ensure that I_{AC} is pulled back to the linear input range of I-ΔΣM. As shown in Fig. 3 (bottom left), the DZ comprises three groups of sampling capacitors and two comparators. During sampling phase (t_1), the bottom plates of all capacitors are shorted to V_{CM} and sample V_{O1}, except C_3 which is reset. In bound comparison phase (t_1+Δt), C_2 and C_6 are tied to V_{UB} and V_{LB}, respectively, to generate upper and lower thresholds (i.e., V_U and V_L) centered at V_{O1}. C_3 is connected to V_{O1} so that V_{DZ} follows V_{O1} with half the amplitude change. Note that C_4 is connected to V_{REF}/V_{REFB} according to the output bit stream (f_{FB}) in each specific cycle. The reasons are twofold. First, V_{DZ}, V_U and V_L experience the same level-shift voltage equal to $-V_{CM}/2$ during bound comparison, as shown in Fig.3(right). Second, since the magnitude, polarity, and integration time of I_{FB} are known, the integration voltage contribution of I_{FB} can be nulled by appropriate V_{REF} and V_{REFB}. Therefore, the change of V_{DZ} is only related to the integration voltage generated by I_{AC}. The comparison result is then added to the previous SZ codes to control the 8b RDAC. It is worth noting that the DZ operates in every I-ΔΣ cycle, but only the first integrator is involved, so it is not limited by the I-ΔΣ loop delay. This way, the DZ can track and remedy an AC input current change up to 1μA/250ns during the entire I-ΔΣM conversion. This feature ensures the DZ track high-frequency current fluctuations beyond the BW of I-ΔΣM.

This LDC chip is implemented in a 0.18μm CMOS process. Fig.4 (top) shows the measured power spectrum density (PSD) with a 1.66μA, 200Hz sinusoidal input, and the SNR/SNDR versus the input current amplitude. With OTA slicing on/off, the SNDR is 94.55/95.74dB and the SNR is 96.01/96.6dB in a 2kHz BW, respectively. Enabling OTA slicing reduces the LDC power from 72μW to 44μW. Fig.4 (bottom left) shows that the SZ can compensate various DC input currents up to 230μA in 8 steps. Fig.4 (bottom right) shows that when SZ is enabled, the maximum DR is extended to 140dB. We performed both chest and wrist PPG tests by using a flexible patch with integrated LEDs and photodiode. Fig.5 (top) shows chest PPG recorded during breathing and breath-holding. The corresponding SpO_2 is derived on the right. Fig.5 (bottom left) shows wrist PPG with the arm raised. Fig.5 (bottom right) shows finger PPG under transient ambient light fluctuations. Thanks to the DZ, the LDC can compensate for rapidly changing currents without saturation.

Fig. 6 compares this work with the recent state-of-the-art LDCs. By utilizing a 2nd-order hybrid I-ΔΣM with SZ and DZ, the highly compact 0.52 mm^2 LDC achieves the highest DR of 140dB in a 2kHz BW and input range of 230μA. Enabling the OTA slicing significantly reduces the LDC power to 44μW, leading to a superior FoM_S=216.5dB. From a system perspective, the LDC supports time-multiplexed input and adaptive LED powering. All these properties make the LDC a serious candidate for high DR light (or current) sensing under highly variable lighting conditions with significant DC and AC contents.

References:

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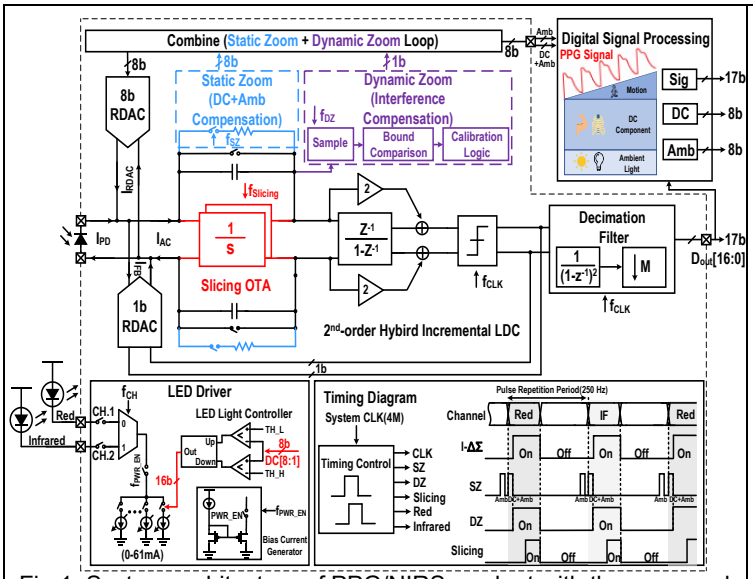

Fig.1: System architecture of PPG/NIRS readout with the proposed I-ΔΣ LDC with slicing OTA and current-mode zoom compensation.

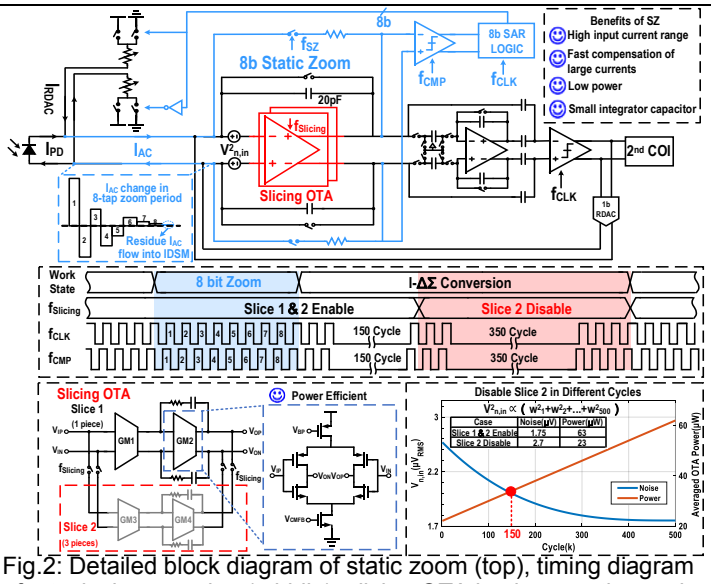

Fig.2: Detailed block diagram of static zoom (top), timing diagram of a typical conversion (middle), slicing OTA implementation and noise/power vs. clock cycle k (bottom).

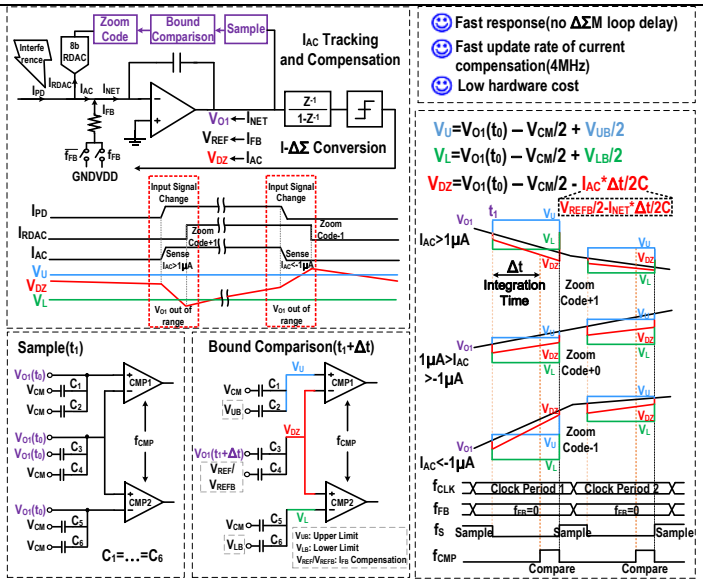

Fig.3: Detailed schematic and operation of dynamic zoom (left), input range identification and timing diagram (right).

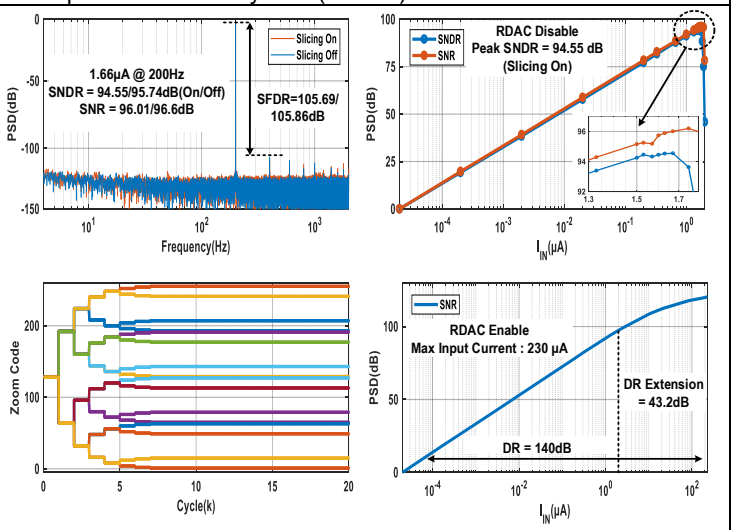

Fig.4: Measurement results: Output PSD when slicing is on/off (top-left); SNR/SNDR vs. input amplitude (top-right). Zoom code of different input DC current up to 230μA (bottom-left). The maximum DR when RDAC is enabled (bottom-right).

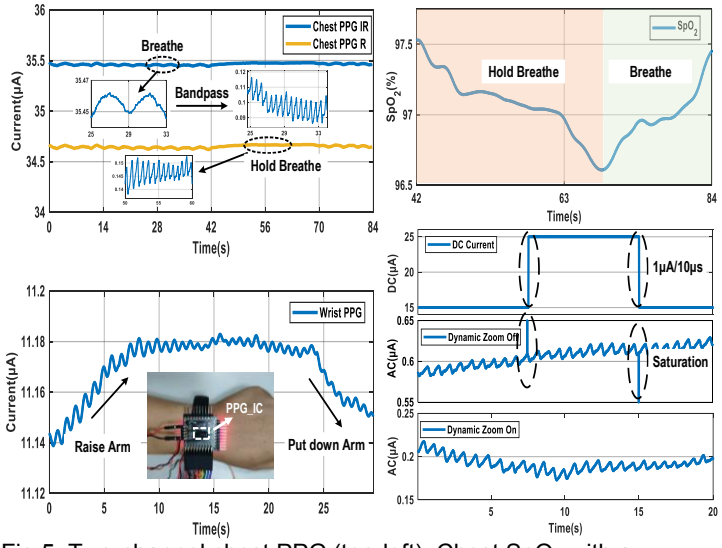

Fig.5: Two-channel chest PPG (top-left). Chest SpO_2 with a controlled breathing (top-right). Wrist PPG with arm raised (bottom-left). Transient responses to fast-varying light (bottom-right).

	ISSCC'20 Marefat	ISSCC'21 Lin[1]	CICC'23 Li[2]	ISSCC'20 Shu	ISSCC'23 Seol[5]	This work	
Technology(nm)	180	180	180	55	180	180	
Area(mm²)	12	8.4	4.6	4.5	0.66	0.52	
Supply(V)	1.5/2.5	1.2/3.3	1.8/3.3	1.8/2.8	1	1.2	
Anti-Interference Scheme	N/A	Threshold filter	Hysteresis Control	Digital TIA	TNS-BS Loop	Dynamic Zoom	
DC Compensation(μA)	51.2(10b)	200(7b)	200(8b)	200(11b)	200(7b)	230(8b)	
Ambient Cancellation(μA)	25.6	50	60	200	200	230	
Max Input(μA)	76.8	200	340	200	200	230	
Noise Bandwidth(Hz)	0.5-10	0.5-20	0.5-20	0.5-20	4k	20	2k
SNDR_AC Path(dB)	70.2	87	94.7	N/A	96.3	104.3	94.5
Max DR(dB)	108.2	134	136.5	130	136.6	151.5	140
AFE Power(μW)	15.7*	28*	30*	72**	64.1**	12.5*	44**
SpO_2 Test (Multi-Channel Operation)	Y	Y	Y	Y	N	Y	
Adaptive LED Control	Y(10b)	N	N	N	N	Y(16b)	
FoMs***	169.2	192.5	194.7	184.4	214.5	213.5	216.5

*. Power measured in PPG Test(duty-cycle mode) **. Power measured in Peak SNDR Input ***. FoMs = DR + 10lg(BW/P)

Fig.6: Performance comparison with the state-of-the-art light (current)-to-digital converters.