An Integrated Burst-Mode 2R Receiver Employing Fast Residual Offset Canceller for XGS-PON in 40-nm CMOS

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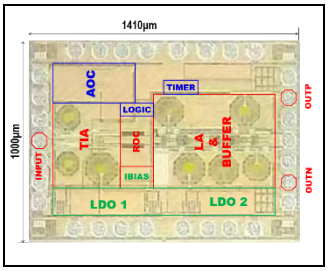
The recent boom of XGS-PON (10Gb/s symmetrical passive optical network) mandates low cost the massive volume of the consumer market. Critically, the time-division multiplexing method in upstream PON demands burst-mode (BM) receiver (Rx) with minimum settling time so that each user can capture more effective bandwidth. The BM-Rx needs to execute the 3R functions of re-amplify (TIA), re-shape (LA) and re-time (CDR) successively. Since the amplitude of the incoming burst signal can vary by more than 1000x from microampere to milliampere, offset cancellation which occurs in the first 2R function tends to be difficult. Made in SiGe BiCMOS, the conventional 2R BM-Rx not only suffer from excessive settling time and large power consumption [1-3], but also are expensive. Some recent CMOS BM-Rx [4,5] have achieved fast settling through high-speed mixed-signal approaches, but their dynamic range, sensitivity and the need of external clocking are incompatible with current PON. In this paper, we present an integrated 2R BM-Rx with fast offset cancellation approaches to reduce the settling time significantly.

Figure 1(a) compares various offset cancellation approaches in the system level. The most adopted AC-coupling approach, which is usually used in discrete form can effectively block the TIA output offset transition, will introduce extra settling time overhead of at least 25ns (5τ) as well as considerable baseline wander due to the direct trade-off between settling time and baseline wander. On the other hand, although the DC coupling itself doesn't introduce extra settling time, the TIA output offset directly feeds to LA, increasing the difficulty and complexity of offset cancellation in LA. Further, it may also encounter the common-mode incompatibility issue in a discrete 2R BM-Rx implementation. We propose a Residual Offset Canceller (ROC), which can achieve fast settling, accurate offset cancellation, small baseline wander all at once with simple design. Shown in Fig. 1(b), the proposed 2R BM-Rx is composed of TIA, S2D (single-to-differential amplifier), ROC, 4-stage LA and Buffer. LDOs, bias, controls and timing circuit are fully integrated on chip, enabling cheap TO-CAN housing commonly employed in PON.

Figure 2 presents the details of the proposed fast BM-TIA automatic offset cancellation (AOC) system. The AOC CTRL module de-activates the AOC loop under small signal burst for high sensitivity. Once started, a three-state AOC approach is executed with its workflow depicted in Fig. 2(a), including coarse AOC, fine AOC and continuous (CM) mode operation. The coarse AOC state is illustrated in Fig. 2(b), where a regulated charge pumping (RCP) approach is used to accelerate charging the gate of the current sink transistor V_{MN1}. By inspection of the extracted instantaneous TIA output DC V_{OUT_DC}, it is decided if the pumping cycle continues until V_{OUT_DC} reaches V_{REF_TIA}. The role of RCP is critical, which not only speeds up the charging drastically, but also takes V_{MN1} to the vicinity of its target state, allowing a follow-up fast small-signal settling in fine analog AOC and AGC, where the loop bandwidth is set large by setting the low pass filter (LPF). Finally, when AOC is settled, the LPF bandwidth is set low, and the AOC loop enters its CM mode for minimum baseline wander. In such a way, the charging of V_{MN1} is dominated by fast charge pumping and additional fast small-signal loop settling. In comparison, the assistant charge pumping (ACP) approach [6] only exercises charge pumping acceleration in a fraction of the settling time, and the intervals between charge pumping is filled with slow large signal slew. From simulation RCP is more than 2x faster than ACP, and more than 7x faster than no-charge pumping approach. Fig. 2(c) shows the simulated TIA AOC behavior with a large 2mApp burst. The total TIA AOC settling time is only 10ns, achieving 1000x acceleration compared to that of a CM-AOC.

Figure 3 details the LA offset cancellation approach and begins by comparison in Fig. 3(a). The conventional feedforward offset cancellation approach generally achieves fast settling due to its open-loop nature. However, the gain mismatch between signal and feedforward path makes it difficult to carry out high-accuracy offset cancelation, which is further exacerbated when multiple LA stages are cascaded. Meanwhile, the feedback offset cancellation approach faces the same trade-off between settling time and baseline wander/accuracy as CM-LA DC offset cancellation (DCOC). To solve the speed-accuracy conundrum, we propose the ROC based time-variant AC-coupling approach, where a small coupling capacitor of 5pF is applied. During TIA AOC settling, the LA input is shorted, which not only suppresses the TIA offset transition, but also incurs negligible settling time overhead t_{ROC} given the small RC constant of 0.5n. When the TIA is settled, the ROC enters its CM mode by restoring the LA input resistance to 400KΩ, which forms a low-frequency cut-off of 80KHz with little baseline wander. Since the ROC virtually doesn't feed offset to LA, it allows the adoption of CM-DCOC loop to only cancel the offset from LA mismatch with high precision, avoiding the accuracy-speed trade-off in most BM-LAs. In sum, the proposed ROC not only achieves fast settling, accurate offset cancellation and small baseline wander at once, but also enables the use of a much simpler CM-DCOC, which greatly reduces the system complexity. Figure 3(b) shows the simulation of BM-Rx with a 2mApp burst. As expected, when ROC settles in 6ns, no more BM AOC is needed in LA. From post-layout simulation, the output offset of the BM-Rx under its whole input range is less than 10mV, with the total Rx settling time less than 16ns.



The 2R BM-Rx is bonded with an off-the-shelf APD and packaged in a 6-pin TO-CAN for time-domain measurement, and the setup is shown in Fig. 4(a). An XGS-PON optical module is used for E/O conversion. The bit error rate (BER) measurement is shown in Fig. 4(b), demonstrating sensitivity of -30.8dBm at BER=1E-3. The 10Gb/s receiver output eyes at various input power are shown in Fig. 4(c), showing sufficient output swing. Figure 5 shows the BM settling behavior, and the settling time is less than 19ns over the whole input optical power range, from -30.8dBm up to -5dBm due to instrument limitation. From the output waveform, we can identify the settling time of TIA is 12ns and ROC settling of 7ns. The 3ns settling time penalty against simulation is due to underestimated parasitic in the timing block.

Figure 6 compares this work with the other reported 1R and 2R BM-Rx for PON. This work achieves settling time 2-10x smaller versus other 1R or 2R BM-Rx. Realized in a single 40nm CMOS chip, the power consumption is 4-8x smaller and die area is also 2-3x smaller, allowing the 2R BM-Rx to be packaged in a TO-CAN used in PON for the first time, which will greatly reduce the cost of both the receiver chip and system package. To the authors' best knowledge, this is the first monolithic CMOS 2R BM-Rx for XGS-PON.

Acknowledgement:

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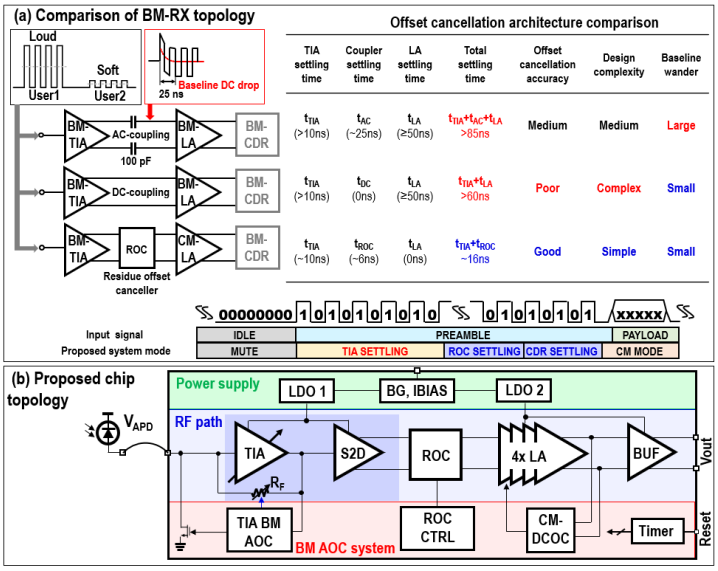

Fig. 1. Offset cancellation architectures and proposed integrated 2R BM-RX.

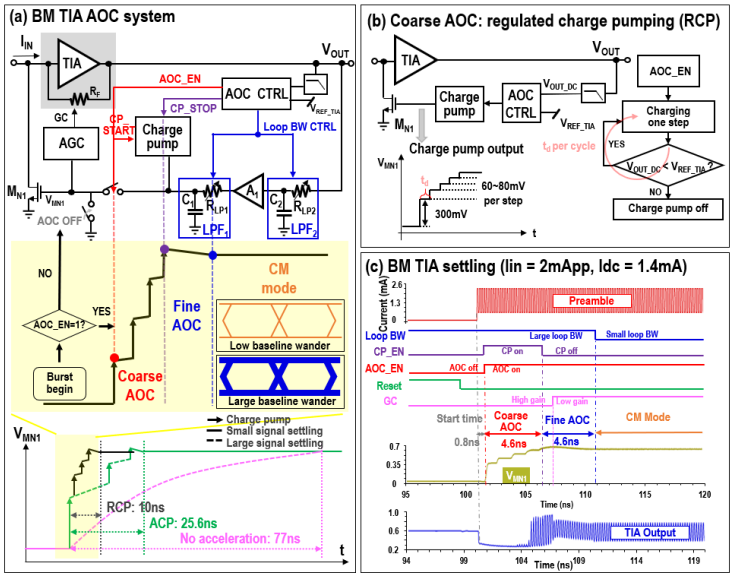

Fig. 2. Proposed fast TIA AOC.

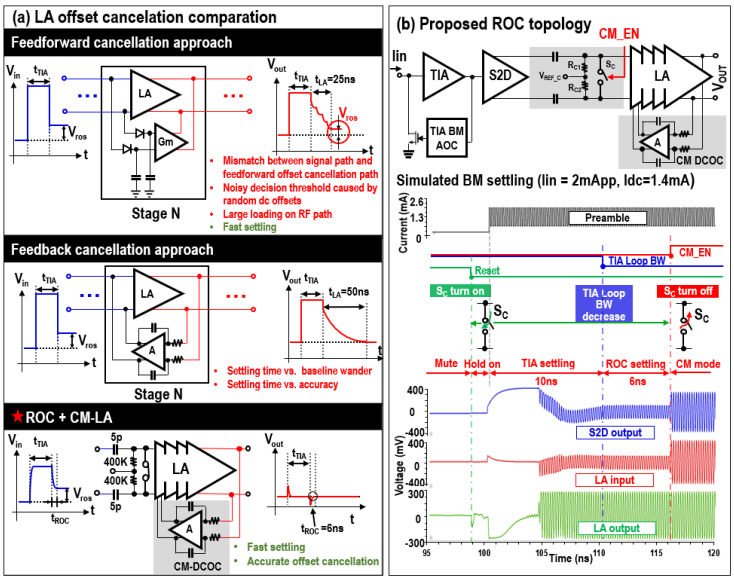

Fig. 3. Proposed ROC and 2R BM-RX settling.

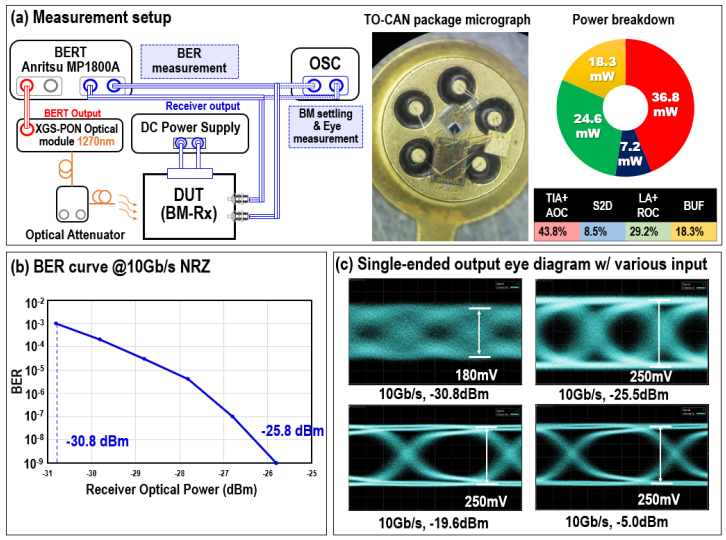

Fig. 4. BER & output eye measurement.

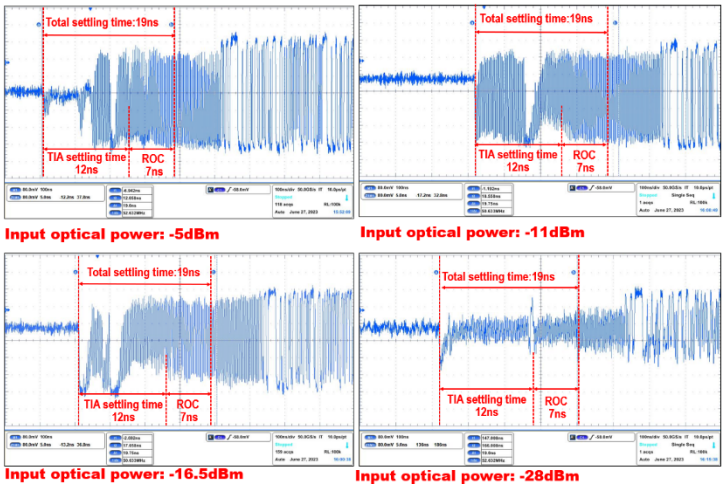

Fig. 5. Rx settling behavior under various Input power.

	[7] OFC 2023	[6] CICC-2022	[1] ISSCC-2012	[2] JLT 2010	[3] JSSC-2013	This work
Data Rate(Gb/s)	25/12.5	10	10	10	10	**10**
Technology	0.13 μm SiGe BiCMOS	40-nm COMS	0.13 μm SiGe BiCMOS	0.18 μm SiGe BiCMOS	250 nm SiGe:C BiCMOS	**40-nm COMS**
Function	1R (Re-amplify)		2R (Re-amplify + Re-shape)			
Integration Method	TIA only		Discrete TIA + LA DC Coupling	Discrete TIA + LA AC coupling	Monolithic TIA + VGA DC coupling	**Monolithic TIA + LA AC coupling**
DC & Gain Settling time(ns)	200	37	75	150	150	**19**
Gain(dBΩ)	58.1	N/A	121	86	85	**93.4**
Noise(pA/√Hz)	N/A	7.9	N/A	N/A	9	**7.9**
Sensitivity (dBm)	-26.3/-26.6 (APD, 1e-2)	-31.5 (APD, 1e-3)	-31.2 (APD, 1e-3)	-29.8 (APD, 1e-3)	-23.2 (PIN,1e-3)	**-30.8 (APD, 1e-3)**
Dynamic Range(dB)	21.5/22.8	25.6	26.2	24.8	22.7	**25.8**
Supply Voltage(V)	N/A	1.6	2.5/2.2	3.3	2.5/3.3	**1.5**
Power(mW)	N/A	66	200(TIA)+430(LA)	300	650	**84**
Die area(mm^2)	N/A	0.90	1.3(TIA)+1.6(LA)	~1(TIA)+4.41(LA)	5.04	**1.41**

Fig. 6. Performance comparison of BM-Rx for PON.