# A direct digitizing, 1MHz bandwidth, 28fA/√Hz current sensing front-end based on a mixed-signal integrator-differentiator TIA in 28nm CMOS

David-Peter Wiens, Ahmed Abdelaal, Bjoern Driemeyer, Joachim Becker, John G. Kauffman, Maurits Ortmanns

Institute of Microelectronics, University of Ulm, Ulm, Germany

Low-noise and high-throughput current sensing front-ends are required for sensor systems such as electrical impedance spectroscopy, ion conductance microscopy, or nanopore-based DNA sequencing [1–3]. Such applications require fA/√Hz noise floor and at the same time hundreds of kHz or even MHz bandwidth (BW).

Fig.1 shows an overview of different current sensing front-ends. Resistive transimpedance amplifiers (R-TIAs) achieve wide BW and low noise, but require a large feedback resistor to maintain a low noise floor [2, 3]. The integrator-differentiator TIA (I-D-TIA) splits the task of low noise (integrator stage) and high BW (differentiator stage) [4–7]. However, the analog differentiator is the dominant power and area consumer due to its high speed requirements and large input capacitor. R-TIA, and I-D-TIA often make use of pseudo resistors, which come with the drawbacks of PVT sensitivity, added shot noise, required precise references and use of silicon-on-insulator (SOI) process. They also require an explicit analog-to-digital converter (ADC) for digitization. While current-mode delta-sigma modulators (CM-DSMs) offer implicit digitization, wide dynamic range, and linearity with high power efficiency. However, they suffer from limited BW due to the required oversampling [1, 8–12].

This work presents a mixed-signal integrator-differentiator TIA (MS-TIA) based on the working principle of the I-D-TIA, where the differentiator and the ADC are exchanged in the signal chain [13] as indicated in Fig.1. It offers the same low noise and high throughput capabilities as the I-D-TIA, but includes digitization and implements more of the signal processing in the digital domain, benefiting from technology scaling.

Fig.2 shows the system architecture of the presented MS-TIA. The input integrator converts the single-ended input current into a differential-ended output voltage via a noiseless feedback capacitor. A continuous-time 3$^{rd}$-order incremental DSM (Inc-DSM) with a 3$^{rd}$-order chain-of-integrator (COI) decimation filter with 20-bit output is used to digitize the integrator output. A similar architecture to that used in [14] was chosen for the Inc-DSM. It operates at a sampling rate of $f_{fast}$=120MHz, is reset at a rate of $f_{slow}$=2MHz, and achieves a SNR/SNDR/SFDR = 78.7/76.1/82.1dB for a 100kHz input tone at -6dBFS input magnitude. The CT ADC allows to omit a switched sampling capacitor and easier drivability. Even though its incremental operation suffers from a noise-penalty of about 2.5dB compared to a free-running DSM as ADC, it allows for multiplexing different integrator frontends in a future multichannel design.

In the AC forward path, the digital output is filtered by a digital differentiator (DDIFF) ($1-z^{-1}$). The DC feedback path is realized by a mixed-signal DC servo loop (DSL) [15]. The incremental ADC output is passed to a digital DSL filter running at $f_{slow}$. Its implementation in the digital domain is advantageous because a low cut-off frequency (<100Hz) is desired, which usually requires large passive components in analog DSLs. In addition the digital DSL filter can be reprogrammed to change the minimum cut-off frequency. The output of the digital DSL filter is passed through a 2$^{nd}$-order digital DSM (DDSM) running at $f_{fast}$ to convert its 14b input into a complementary 1b output. The large high-frequency digital quantization noise of the DDSM is filtered by a single operational amplifier (OA) second-order analog low-pass filter (LPF) (see Fig.3). The feedback current of the DSL in Fig. 2 is generated by an active voltage-to-current converter (V2I) shown in detail in Fig.3. The current generated across the input resistor $R_{in}$ is damped by the capacitor ratio $C_d/C_i$. To avoid saturation of the active current damper, a bias resistor is used in parallel with $C_i$, which is 10x larger than $R_{in}$. To bypass the bias resistor and the resulting noise, the slowly changing input of the V2I is modulated with chopper switches to a higher frequency, where the impedance of $C_i$ is significantly reduced compared to $R_{bias}$. The output current is generated through the capacitor $C_d$ and then demodulated. The proposed V2I generates a precise current in the nA range without using pseudo-resistors.

Fig.4 shows the measurement results of the presented MS-TIA. The total noise of high-BW TIAs is very sensitive to the input capacitive load. The lowest noise is thus achieved with a floating input and the measured integrated noise is 131pA$_{rms}$ over a BW of 1MHz, with an estimated parasitic capacitance of 1.1pF (from the ESD protection and bond pad). A minimum spot noise of 22fA/√Hz is measured. A constant total noise of 185pA$_{rms}$ and a minimum spot noise of 28fA/√Hz are measured over various DC inputs (max ±12nA). The DC input is generated via an off-chip 100MΩ resistor. Compared to the measurements with a floating input, the parasitic capacitance increased by roughly 1pF due to the connections to the PCB and the off-chip resistor.

Fig.4 also shows two output spectra for two distinct input tones at 100kHz and 800kHz, respectively. The AC input is generated via the coupling capacitance of adjacent PCB traces (approximately 500fF). For a 100kHz input tone, a maximum SNR/SNDR/SFDR = 46.5dB/44.2dB/48.8dB was measured, while for an 800kHz tone a maximum SNR/SNDR/SFDR = 59.4dB/58.2dB/64.0dB was obtained. Due to the frequency dependent dynamic range (DR) of the input integrator within the MS-TIA, similar to I-D-TIA [4], the low frequency input achieves a lower maximum SNR. The transimpedance of the MS-TIA is measured with different minimum cut-off frequencies, which can in fact be changed by two orders of magnitude by reprogramming the digital DSL filter. The MS-TIA achieves a flat transimpedance gain of $R_{TIA}=T_S/C_i$=126dBΩ. The gain of the MS-TIA decreases at higher frequencies due to the decreasing signal gain of the Inc-DSM and the simple DDIFF used to compensate for the analog integrator. This could be alleviated by using an oversampled DDIFF or an equalizing filter flattening the frequency response, but also increasing the bandedge noise.

Fig.5 shows a DR sweep for two different input tones, 100kHz and 800kHz. Due to the frequency dependent DR of the input integrator the higher frequency input tone has a higher DR. However, due to the reduced gain of the MS-TIA towards the band edge, at small input amplitudes, the DR curve of the 800kHz input tone is shifted to the right compared to the 100kHz input tone. A total harmonic distortion (THD) sweep for a 100kHz input tone is also shown in Fig.5. A deep in-band tone was chosen for the THD measurement because all relevant harmonics are within the first nyquist zone.

The MS-TIA was fabricated in a 28nm CMOS process, occupying an area of 0.13mm$^2$ and consuming 8.9mW of power including digitization. The ADC and the input integrator each consume almost half of the power while the ADC dominates the area consumption. The power and area required by the analog part of the DSL, i.e. the LPF and V2I, plays only a minor role. The area and power required by the digital part of MS-TIA, specifically COI, DSL filter, and DDSM, is negligible due to the advanced process node.

Fig.6 shows the $FOM_{noise}$ of different current sensing front-ends over a wide BW range. At the realized bandwidth, the presented MS-TIA achieves a compatible $FOM_{noise}$ compared to purely analog front-ends (R-TIA and I-D-TIA) which miss the digitiziation. Compared to digitizing current sensing frontends (CM-DSM) it achieves orders of magnitude higher BW. Furthermore the presented MS-TIA achieves a competitive $FOM_{Schreier}$ among other current sensing frontends.

In Fig.6, the MS-TIA is compared to the state of the art. Unlike most of the other implementations shown, the low noise floor achieved by the MS-TIA is maintained regardless of the DC input. In conclusion, this work extends currently existing purely analog low noise and high BW front-ends by implementing more of the signal processing tasks in the digital domain, taking advantage of efficient realization in advanced process nodes.

2025 IEEE Custom Integrated Circuits Conference (CICC) | 979-8-3315-1745-8/25/$31.00 ©2025 IEEE | DOI: 10.1109/CICC63670.2025.10983397

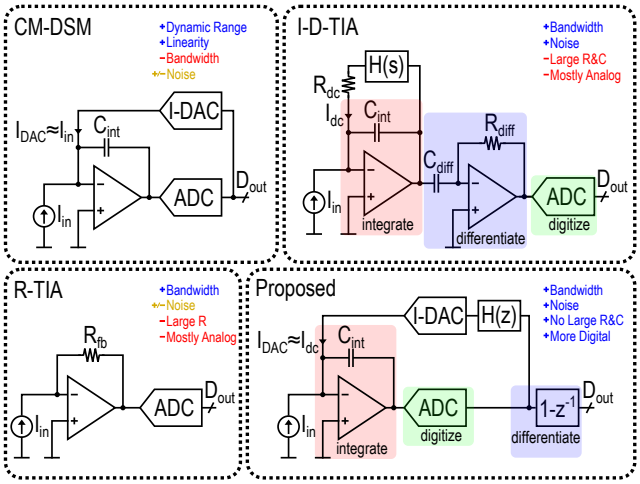



Fig. 1. Conceptual overview of prior works: resistive TIA (bottom left), current-mode DSM (top left), integrator-differentiator TIA (top right), and the proposed mixed-signal integrator-differentiator TIA (bottom right).

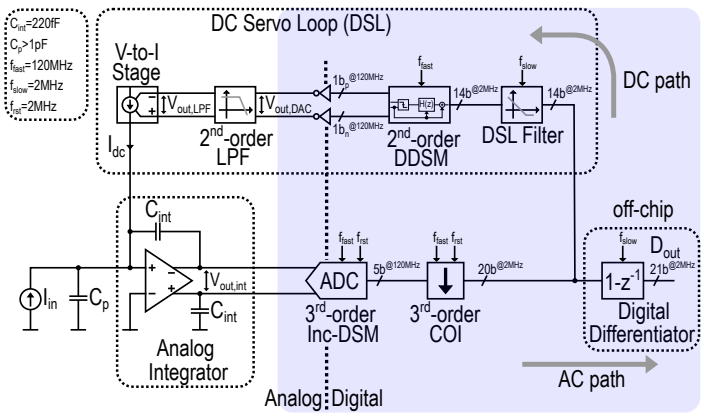



Fig. 2. Architecture of the proposed MS-TIA. As the DDIFF is placed off-chip for flexibility, it was synthesized in the technology used. After place and route it requires 50µW of power and 644µm$^2$ of area, both below 1% of the overall area/power budget.

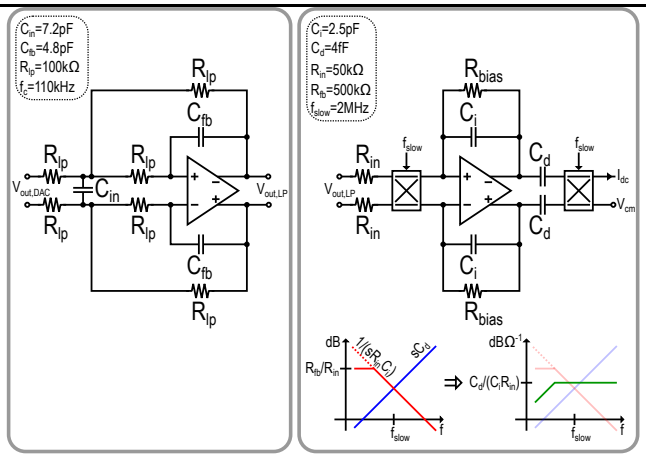


Fig. 3. LPF used inside the DSL (left). The LPF has a cut-off frequency of $f_c$=110kHz. Due to the fast clock rate of the DDSM, the cut-off frequency of the LPF can be relatively high, thus requiring smaller R and C components. V2I stage generating the DC feedback (right).

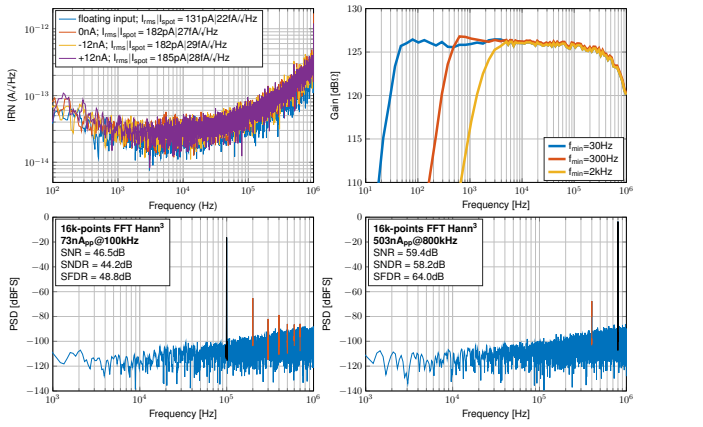


Fig. 4. Input referred noise of the MS-TIA with floating input, and with different DC inputs (top left). Transfer behavior of the MS-TIA for different settings inside the DSL filter (top right). Output spectra of the MS-TIA with in-band 100kHz input sinusoidal (bottom left), and band-edge 800kHz input sinusoidal (bottom right).

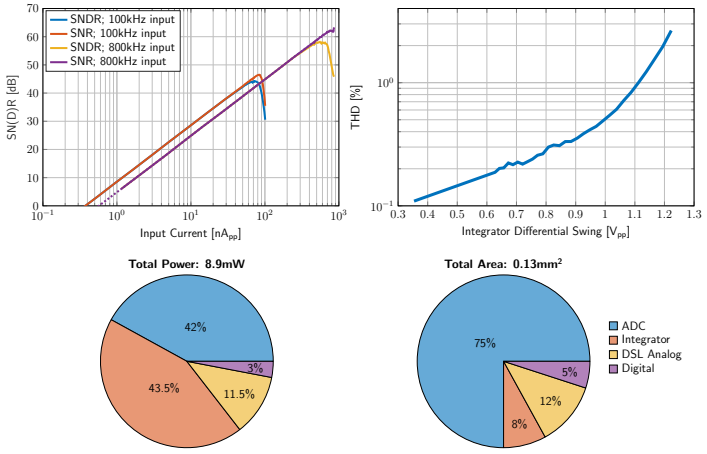



Fig. 5. Dynamic range of the MS-TIA for two different input tones (top left), and THD of the MS-TIA for a 100kHz input tone (top right). Power and Area breakdown (bottom).

| | This work | TBCAS'16[5] | TVLSI'17[6] | JSSC'18[2] | TCASI'22[7] | ISSCC'23[11] |
|---|---|---|---|---|---|---|
| Technology | **28nm** | 180nm | 130nm | 180nm SOI | 180nm SOI | 180nm |
| Topology | **MS-TIA** | I-D-TIA | I-D-TIA | R-TIA | I-D-TIA | CM-DSM |
| Supply [V] | **0.95** | 1.8 | 3.3 | 1.8 | 1.8 | 1.0 |
| Area [mm$^2$] | **0.13** | 0.091 | 0.2 | 0.09 | 0.43 | 0.66 |
| Power [W] | **8.9m** | 5.2m | 30m | 9.3m | 27m | 64µ |
| Bandwidth [Hz] | **1M** | 2M | 1M | 2M | 7.7M | 4k |
| Resolution [$A_{rms}$] | **131p** | 100p[b] | 52p | N.A. | 440p | 29p |
| Min. Noise [A/√Hz] | **28f** | 12f[c] | 10f[c,d] | 120f[d] | 1.6f[c] | 460f[c] |
| SNDR [dB] | **58** | 35.2 | N.A. | N.A. | N.A. | 96 |
| THD [%] | **0.4[a]** | N.A. | 3[e] | 3[a] | 0.5[a] | N.A. |
| Digital Output | **Yes** | No | No | No | No | Yes |

[a] @-6dBFS swing [b] @integrated over 1MHz BW [c] @0DC input [d] estimated from plot [e] @ <0.4V swing

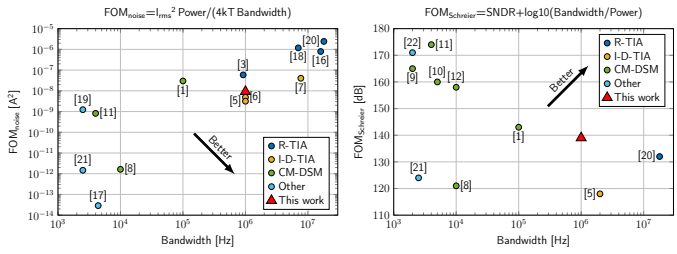
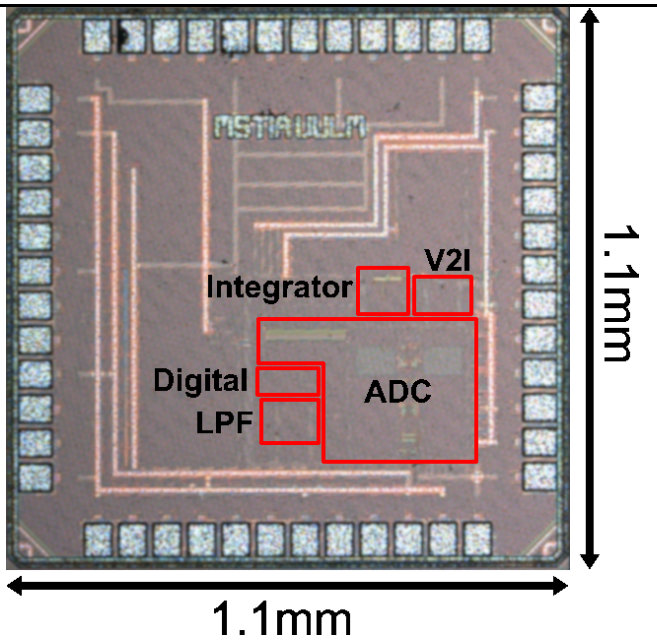



Fig. 6. Comparison between the presented and prior work.



Die micro-graph

**Acknowledgements:**

This work was funded by the German Federal Ministry of Education and Research through the Project VE-FIDES under Grant 16ME0258.

**References:**

[1] M. Rajabzadeh et al, "An Integrated Readout for Current Sensing Based on a $\Sigma\Delta$ Modulator with Switched Capacitor Feedback", ESSCIRC, 2019, DOI: 10.1109/ESSCIRC.2019.8902914

[2] D. Djekic et al, "A 0.1% THD, 1-M$\Omega$ to 1-G$\Omega$ Tunable, Temperature-Compensated Transimpedance Amplifier Using a Multi-Element Pseudo-Resistor", JSSC, 2018, vol. 53, issue 7, pp. 1913-1923, DOI: 10.1109/JSSC.2018.2820701

[3] A. Das et al, "A 376$\mu$W per-channel, Drift-tolerant Translocation Recording Frontend with Event Detection for Nanopore Sensor Arrays", ESSCERC, 2024, DOI: 10.1109/ESSERC62670.2024.10719545

[4] G. Ferrari et al, "Transimpedance Amplifier for High Sensitivity Current Measurements on Nanodevices", JSSC, 2009, vol. 44, issue 5, pp. 1609-1616, DOI: 10.1109/JSSC.2009.2016998

[5] S. Dai et al, "A 155-dB Dynamic Range Current Measurement Front End for Electrochemical Biosensing", TBCAS, 2016, vol. 10, issue 10, pp. 935-944, DOI: 10.1109/TBCAS.2016.2612581

[6] M. Taherzadeh-Sani et al, "A 170-dB$\Omega$ CMOS TIA With 52-pA Input-Referred Noise and 1-MHz Bandwidth for Very Low Current Sensing", TVLSI, 2017, vol. 25, issue 5, pp. 1756-1766, DOI: 10.1109/TVLSI.2017.2654452

[7] M. Haeberle et al, "An Integrator-Differentiator Transimpedance Amplifier Using Tunable Linearized High-Value Multi-Element Pseudo-Resistors", TCAS-I, 2022, vol. 69, issue 8, pp. 3150-3163, DOI: 10.1109/TCSI.2022.3174174

[8] M. Amayreh et al, "A Fully Integrated Current-Mode Continuous-Time Delta-Sigma Modulator for Biological Nanopore Read Out", TBCAS, 2019, vol. 13, issue 1, pp. 225-236, DOI: 10.1109/TBCAS.2018.2889536

[9] S.-H. Wu et al, "A Current-Sensing Front-End Realized by A Continuous-Time Incremental ADC with 12b SAR Quantizer and Reset-Then-Open Resistive DAC Achieving 140dB DR and 8ppm INL at 4kS/s", ISSCC, 2020, DOI: 10.1109/ISSCC19947.2020.9062990

[10] M. ElAnsary et al, "50nW Opamp-Less $\Delta\Sigma$-Modulated Bioimpedance Spectrum Analyzer for Electrochemical Brain Interfacing", JSSC, 2020, vol. 55, issue 7, pp. 1971-1983, DOI: 10.1109/JSSC.2020.2981033

[11] T. Seol et al, "A 1V 136.6dB-DR 4kHz-BW $\Delta\Sigma$ Current-to-Digital Converter with a Truncation-Noise-Shaped Baseline-Servo-Loop in 0.18$\mu$m CMOS", ISSCC, 2023, DOI: 10.1109/ISSCC42615.2023.10067537

[12] S.-Y. Lee et al, "A Direct Current-Sensing VCO-Based 2nd-Order Continuous-Time Sigma-Delta Modulator for Biosensor Readout Applications", TBCAS, 2024, vol. 18, issue 2, pp. 288-298, DOI: 10.1109/TBCAS.2023.3322901

[13] D.-P. Wiens et al, "A Mixed-Signal Integrator-Differentiator-TIA", TCAS-II, 2024, vol. 71, issue 3, pp. 1057-1061, DOI: 10.1109/TCSII.2023.3318725

[14] M. A. Mokhtar et al, "A 0.9-V DAC-Calibration-Free Continuous-Time Incremental Delta-Sigma Modulator Achieving 97-dB SFDR at 2 MS/s in 28-nm CMOS", JSSC, 2022, vol. 57, issue 11, pp. 3407-3417, DOI: 10.1109/JSSC.2022.3160325

[15] C.-L. Hsu et al, "A Hybrid Semi-Digital Transimpedance Amplifier With Noise Cancellation Technique for Nanopore-Based DNA Sequencing", TBCAS, 2015, vol. 9, issue 5, pp. 652-661, DOI: 10.1109/TBCAS.2015.2496232

[16] M. Tan et al, "A Front-End ASIC With High-Voltage Transmit Switching and Receive Digitization for 3-D Forward-Looking Intravascular Ultrasound Imaging", JSSC, 2018, vol. 53, issue 8, pp. 2284-2297, DOI: 10.1109/JSSC.2018.2828826

[17] G. Mulberry et al, "Analysis of Simple Half-Shared Transimpedance Amplifier for Picoampere Biosensor Measurements", TBCAS, 2019, vol. 13, issue 2, pp. 387-395, DOI: 10.1109/TBCAS.2019.2897287

[18] E. Kang et al, "A 2pA/$\sqrt{}$Hz Transimpedance Amplifier for Miniature Ultrasound Probes with 36dB Continuous-Time Gain Compensation", ISSCC, 2020, DOI: 10.1109/ISSCC19947.2020.9063052

[19] J.-C. Chien et al, "Design and Analysis of a Sample-and-Hold CMOS Electrochemical Sensor for Aptamer-Based Therapeutic Drug Monitoring", JSSC, 2020, vol. 55, issue 11, pp. 2914-2929, DOI: 10.1109/JSSC.2020.3020789

[20] M. Zhou et al, "An RX AFE With Programmable BP Filter and Digitization for Ultrasound Harmonic Imaging", TBCAS, 2022, vol. 15, issue 6, pp. 1430-1440, DOI: 10.1109/TBCAS.2021.3135859

[21] I. Mostafa et al, "A 2.2 fA/$\sqrt{}$Hz, 120 dB Dynamic Range, 12 G$\Omega$ Hybrid Readout Interface for Various Ionic Spectroscopy Applications", ESSCIRC, 2023, DOI: 10.1109/ESSCIRC59616.2023.10268698

[22] Y. Chang et al, "A 44$\mu$W 140dB-DR Hybrid Light-to-Digital Converter with Current-Tracking Dynamic Zoom and Power-Scaling OTA", CICC, 2024, DOI: 10.1109/CICC60959.2024.10529087