A Low-Power, Compact, Adaptive Logarithmic Transimpedance Amplifier Operating over Seven Decades of Current

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***Abstract*— This paper describes a transimpedance amplifier using logarithmic compression of the input current for wide dynamic range current sensing applications. Measurements demonstrate operation over currents ranging from 200fA to 2μA with an average error of 0.8%. It is analytically shown that the power dissipation of the non-adaptive structure varies linearly with dynamic range. This amplifier alleviates this strong dependance on dynamic range and achieves low-power operation by adapting the bias current of the amplifier depending on input current thus burning an average power of 3.45μW per decade of current. Either SNR or Bandwidth can be made to trade-off with the input current depending on application. If the bandwidth is limited to 5kHz, it achieves an average SNR of 65dB.**

I. Transimpedance Amplifiers

Transimpedance amplifiers (TIA) are used in a wide variety of applications ranging from microsystem sensors to optical preamplifiers. Important specifications for such amplifiers include bandwidth, power dissipation, input-current noise, and area. The trade-offs among these parameters are particularly exacerbated in applications requiring very high dynamic ranges, like sensing and reprogrammable systems. Sensing systems interface the physical world which is inherently highly dynamic, while reprogrammable systems must also cater to a wide variety of applications and specifications.

Logarithmic compression of the current using a MOSFET in subthreshold has been explored to solve the issue of obtaining a wide dynamic range [1], [2]. For proper phase margin, all of these approaches assume that the poles of the amplifier are sufficiently higher than the dominant pole set by the feedback element. However, satisfying this assumption entails burning considerable power in the amplifier to push the pole away from the maximum input pole set by the highest input current. A solution where the bias current of the amplifier is adjusted has been proposed in [3]. But the adaptation loop requires a large off-chip capacitor for stability and also degrades the SNR of the system. In this paper, we analyze in detail the trade-offs involved in a power efficient design of such a system and propose an adaptation method to accomplish the same.

In section II, a small-signal analysis of the TIA is shown along with an analysis of the power dissipation constraints. Section III introduces an adaptation strategy to stabilize the circuit for wide range of input currents while maintaining low-power operation. The advantage of this method in terms of power dissipation is analyzed. Section IV discusses the noise performance of the circuit showing trade-off between bandwidth and SNR. Finally, we draw conclusions in the last section.

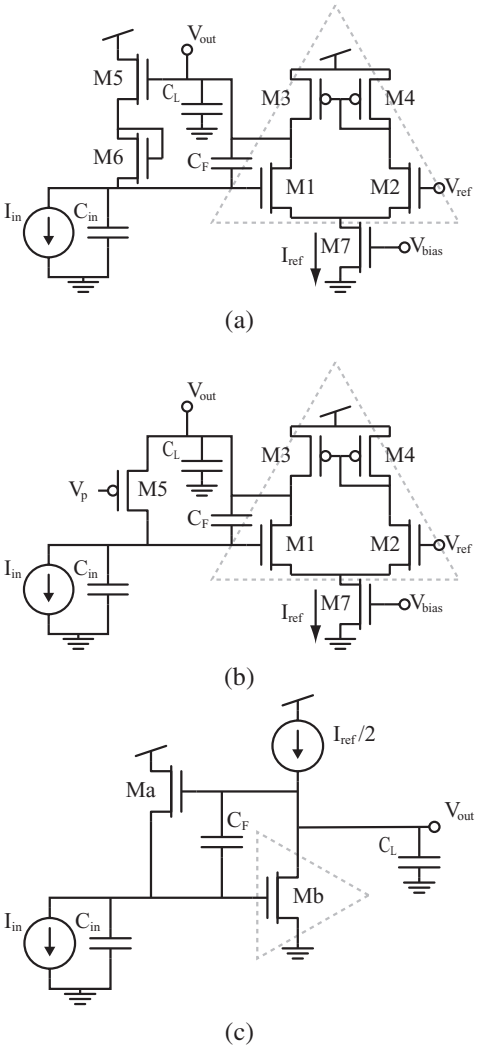

Fig. 1: **Logarithmic Transimpedance Amplifier:** (a) Common-drain configuration (b) Common-gate configuration (c) Simplified small-signal model of (a)

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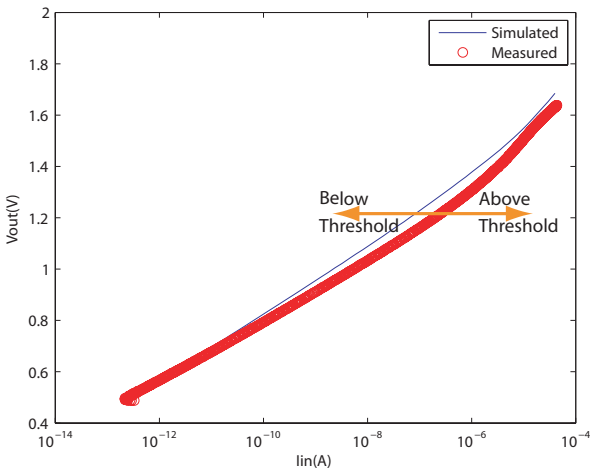

Fig. 2: **Current-Voltage characteristics:** Measured and simulated current to voltage curves at DC. At higher currents, the slope becomes steeper because of the MOSFET entering above threshold region from sub-threshold.

II. Logarithmic Transimpedance Amplifier: Topologies

Figures 1(a) and (b) depict the structure of common-drain and common-gate logarithmic TIAs. In both cases, the logarithm is obtained due to the exponential I-V relation of a MOS in sub-threshold, while the amplifier speeds up the response by holding the input node fixed. As the operation of both is very similar, we shall focus our discussion on the common-drain one, while pointing out important differences when necessary.

In fig. 1(a), transistors M1 - M4, form a basic differential amplifier with M7 as the current source. M5 and M6 form the feedback element. M5 and M6 form an equivalent transistor with an effective κ lesser than that of a single transistor, where κ is the inverse of the subthreshold slope factor [4]. This helps in increasing the sensitivity. The DC output voltage can be expressed as:

$$V_{\rm out} = \frac{V_{\rm ref}}{\kappa^2} + \frac{U_{\rm T}}{\kappa_{eff}} ln\left(\frac{I_{\rm in}}{I_{\rm n}}\right), \quad (1)$$

where $U_{\rm T}$ is the thermal voltage and $I_{\rm n}$ is the pre-exponential factor in the I-V relation of a sub-threshold NMOS.

A version of this circuit was designed in 0.5μm CMOS. Figure 2 shows the measured and simulated current voltage relation with both curves showing good correlation. A curve fit to this plot for currents ranging from $200fA$ to $2\mu A$ gives a linear slope of 0.55, which translates to κ_{eff}=0.47.

A. Small-signal Analysis

To generate a small signal transfer function for the structure, Figure 1(c) can be used. It is to be noted that Mb in 1(c) represents the amplifier, while Ma in 1(c) represents M5 and M6 in Fig. 1(a) and has an effective degenerate $G_{\rm ma}$ given by $\kappa G_{\rm m5}/(\kappa+1)$ which actually encodes the effect of κ_{eff}. Analyzing Fig. 1(c), we get the poles of the circuit for two particular cases of interest:

CASE I : $C_{\rm IN} >> C_{\rm F}$

This is the most frequently encountered scenario when the input capacitance dominates the frequency response. Using dominant pole approximation and noting that $G_{\rm mb} >> G_{\rm ma}$, the poles are given by:

$$p_1 \approx -\frac{AG_{\rm ma}}{C_{\rm IN}} \quad ; \quad p_2 \approx -\frac{G_{\rm ob}}{C_{\rm F}+C_{\rm L}}. \quad (2)$$

CASE II : $C_{\rm F} >> C_{\rm IN}$

In this case, the input capacitance is so small that generally an explicit $C_{\rm F}$ is needed to robustly design the input pole. In this case:

$$p_1 \approx -\frac{G_{\rm ma}}{C_{\rm F}} \quad ; \quad p_2 \approx -\frac{G_{\rm mb}}{C_{\rm IN}+C_{\rm L}}. \quad (3)$$

The value of p_1 can be intuitively computed by noting that the total capacitor at input, $C_{\rm tot}$ and the input impedance, $Z_{\rm in}$ are given by:

$$C_{\rm tot} = C_{\rm IN} + AC_{\rm F} = A \times C_{\rm eff} \quad ; \quad Z_{\rm in} \approx \frac{1}{AG_{\rm ma}}, \quad (4)$$

where A is the gain of the amplifier.

From the above analysis we see that p_1 depends on the input current and moves to higher frequencies as the input current increases.

The small signal analysis for the common-gate is very similar to the one outlined above. The significant difference is that in the common drain configuration, the $C_{\rm GS}$ of $M_{\rm a}$ is the minimum value of $C_{\rm F}$, which gets Miller multiplied by the gain of the amplifier. This inherently sets a limit on the maximum bandwidth attainable ($f_{\rm t}$) at a particular input current. So if the desired bandwidth is larger than this, the only option is the common gate topology.

B. Power Dissipation Limits

In this text, minimizing power dissipation is used synonymously with minimizing $I_{\rm ref}$, the bias current of the amplifier. It is assumed that $I_{\rm ref}$ flows through M7 in Fig. 1 (b). κ is assumed to be 1 for simplicity. It is also assumed that typically $C_{\rm IN} >> C_{\rm F}$ unless otherwise mentioned. Also, the desired bandwidth, minimum and maximum input currents are denoted by BW, $I_{\rm in,min}$ and $I_{\rm in,max}$ respectively.

The conditions constraining $I_{\rm ref}$ are bandwidth>BW and phase margin>45° for all currents. As the minimum bandwidth occurs when the input current is minimum, it is sufficient to ensure that the bandwidth at minimum input current is larger than BW. Thus we need,

$$\frac{AI_{\rm in,min}}{C_{\rm IN}U_{\rm T}} > BW, \quad (5)$$

where it is assumed that $C_{\rm F} < C_{\rm IN}/A$. (5) defines the minimum gain needed to meet the bandwidth specification. The second equation comes from the phase margin specification:

$$p_{2,\rm OPENLOOP} > BW_{\rm max} = \frac{AI_{\rm in,max}}{C_{\rm IN}U_{\rm T}}. \quad (6)$$

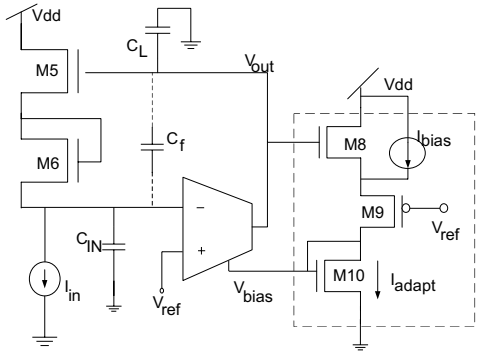

Fig. 3: **Adaptation:** Circuit to adapt the amplifier's bias current based on input.

Thus the power dissipation of the amplifier can be found by considering it to be proportional to the gain-bandwidth product as:

$$I_{ref} > \frac{U_T^2 C_L C_{IN} (BW)^2 DR}{I_{in,min}}, \tag{7}$$

where DR is the dynamic range or ratio of maximum and minimum input currents. The power can be seen to be proportional to dynamic range, input and output capacitances and square of bandwidth. The analysis of the other structure exactly follows that of its common drain counterpart. The small signal analysis sets a minimum requirement on $I_{\rm b}$, the current flowing through the amplifier transistor $M_{\rm b}$. However, since the input current is sourced from the same current supply as the amplifier, $I_{\rm ref}$ must be larger than the maximum possible input current $I_{\rm in,max}$, i.e.:

$$I_{ref} = I_{in,max} + I_{b,max}. \tag{8}$$

Hence the common drain is always more power efficient than the common gate as $I_{\rm in,max}$ is orders of magnitude larger than $I_{\rm in,min}$ for wide dynamic ranges.

III. Adaptation in the Logarithmic Amplifier

Fig. 3 depicts the schematic of the bias current adaptation method. Transistors M8 and M9 replicate $I_{\rm in}$ to produce the adaptive current $I_{\rm adapt}$. M9 acts as a follower to hold the source of M8 constant. In a small-signal sense, the source of M8 sees an impedance of $1/G_{\rm m9}$. The current through M10 is mirrored with a gain of K $\sim$ 10. To find an expression for $I_{\rm adapt}$, we equate the currents through M8 and M9 to obtain:

$$I_{\rm adapt} = K I_{\rm in} e^{((1-\kappa)V_{\rm ref} - \alpha)/((1+\kappa)U_{\rm T})}, \tag{9}$$

where α is given by $U_{\rm T}\ln(I_{\rm n}/I_{\rm p})$ and other symbols are as previously described. The adaptation circuitry moves p_2 by increasing the tail current of the differential amplifier. A current source is added parallel to M8 to ensure that a minimum bias current always flows through the differential pair. The loop-gain of this adaptation loop is very low due to the high CMRR of the amplifier and thus there is no possibility of instability. Another attractive property of this adaptation is that any noise contributed by the transistors M8 - M10 is rejected by the CMRR. The bandwidth of the adaptation loop

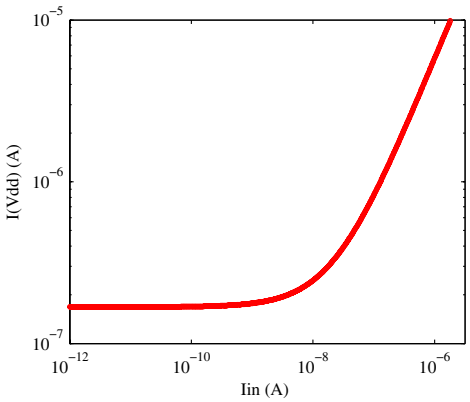

Fig. 4: **Bias current adaptation:** Measured current drawn from the power supply demonstrating adaptation of the amplifier bias.

is set by the sum of $I_{\rm in}$ and the fixed bias current. In this implementation, p_1 is always the dominant pole. Consequently bandwidth scales linearly with $G_{\rm m5}$ and thus linearly with $I_{\rm in}$ when M5 is in sub-threshold. Figure 4 demonstrates measured adaptation of the bias current of the amplifier. From this curve, the average power consumed from the 3.3V power supply is 3.45μW.

A. Power Dissipation

The first constraint based on bandwidth requirement is same as (5). For the second constraint, we know that $I_{\rm ref}$ in this case is variable (as it is adapting) and relate it to the value of $I_{\rm in}$:

$$p_{2,\rm OPENLOOP} \geq \frac{A I_{\rm in}}{C_{\rm IN} U_{\rm T}}, \tag{10}$$

where the symbols used were introduced in the last section on power dissipation. Similar to previous sections, the power is found by considering it proportional to gain-bandwidth as:

$$I_{\rm ref} > \frac{U_{\rm T}^2 C_{\rm L} C_{\rm IN} (BW)^2 I_{\rm in}}{I_{\rm in,min}^2}. \tag{11}$$

In order to find the average power dissipation it should be noted that due to the nature of the data (varying over decades), the geometric mean is the proper measure of average. Therefore,

$$I_{\rm ref}(avg) = \frac{U_{\rm T}^2 C_{\rm L} C_{\rm IN} (BW)^2 \sqrt{DR}}{I_{\rm in,min}}. \tag{12}$$

Thus comparing (7) and (12) we see that adaptation improves the power dissipation by a factor of square root of dynamic range which can be as large as thousand for a system operating over six decades of current. For the common gate, the gains achieved by adaptation are also sizable because it replaces $I_{\rm in,max}$ in (8) with $I_{\rm in}$.

IV. Noise Performance of the Adaptive Logarithmic TIA

For the noise analysis, we consider channel noise current sources, $\tilde{i}_k^2$ for transistor Mk, and compute their contribution to voltage noise power, $\hat{V}_{\rm out}^2$ at the output. The calculation can be simplified by noting that noise currents due to transistors

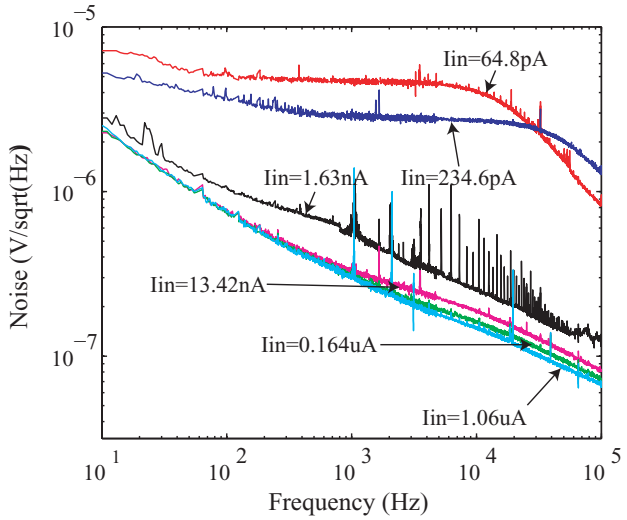

Fig. 5: **Noise performance:** Measured output voltage noise spectrum.

M7 - M10 appear as a common mode signal to the differential amplifier and are attenuated by the CMRR. Also, M5 and M6 are in saturation with equal values of $G_{\rm m}$ denoted by $G_{\rm m5}$ in the following analysis. Then we have an input referred current noise whose value is given by:

$$\hat{i}_{in}^2 \approx \left(\frac{\kappa}{\kappa+1}\right)^2 (\tilde{i}_5^2 + \tilde{i}_6^2) + \left(\frac{\kappa}{\kappa+1}\frac{G_{\rm m5}}{G_{\rm m1}}\right)^2 (\sum_{k=1}^{4} \tilde{i}_k^2) \quad (13)$$

From (13) it is evident that as the adaptation makes $G_{\rm m1} >> G_{\rm m5}$, the noise due to the amplifier becomes negligible. The noise at the output is going to have a thermal noise component and a component due to 1/f noise. This expression needs to be integrated over the bandwidth of the TIA to get the total integrated output noise. For the analytic derivation, we only consider the thermal noise component of a transistor. Using the transfer function from $I_{\rm in}$ to $V_{\rm out}$ calculated earlier, we get the total noise to be:

$$\hat{V}_{\rm out,total}^2 = \frac{4qI}{G_{\rm m5}^2}\int \frac{df}{1+\frac{\omega^2}{p_1^2}} = \frac{kT}{(\kappa+1)C_{\rm eff}} \quad (14)$$

Thus the total integrated noise is independent of I, a result that is expected because the bandwidth increases with I while the voltage noise density at the output decreases with I.

The output voltage noise spectrum limited to 100kHz was measured using a spectrum analyzer(Stanford research System's SR 780) for different input currents. The result is plotted in Fig. 5. The bandwidth obtained from the noise plots corroborate the value of $C_{\rm eff}$≈20fF, which is close to the value calculated based on process parameter values for a 0.5μm AMI process. The theoretically calculated thermal noise density for $I_{\rm in}$ = 65 pA including shot noise of the source is around 6μV which matches with the measured noise density. The SNR can now be computed using the transfer function as follows:

$$SNR_{\rm power} = \frac{(\kappa+1)^3}{\kappa^4}\frac{C_{\rm eff}U_{\rm T}}{q} \quad (15)$$

But it should be noted that in applications like floating-gate programming or imaging, the scaling of bandwidth with input current, as is obtained here, is not required. Rather, this system demands a constant bandwidth of a few kHz depending on a fixed sample rate of the system clock. Thus using a filter after the TIA to limit the bandwidth, we get the SNR to scale with I_{in}. The SNR in the case where the bandwidth is limited to "f_{BW}" is given by:

$$SNR_{power} \approx \left(\frac{\kappa+1}{\kappa}\right)^2 \frac{I_{in}}{qf_{BW}} \quad (16)$$

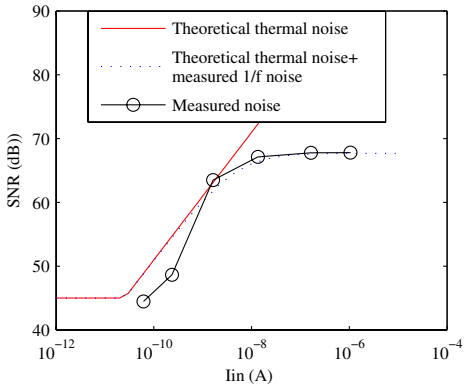

Fig. 6: **Signal to noise ratio:** Scaling of SNR with input current for a fixed bandwidth of 5kHz.

Fig. 6 depicts the theoretically predicted and the measured variation of SNR for f_{BW} equal to 5kHz. Over the plotted range of input currents the average SNR is approximately 65dB. It should be noted that the increase in SNR with increasing current saturates for the measured case, because the contribution of 1/f noise starts dominating in the 5kHz band.

V. Conclusions

In this paper, we present the two major topologies for a transimpedance amplifier using log-compression operating over a large current range. We analyze in detail the power dissipation for these structures and show their functional dependance on speedup (BW/$I_{in,min}$), dynamic range ($I_{in,max}/I_{in,min}$) and input, output capacitances. An adaptation method, modifying the amplifier's bias current depending on input current, to maintain bandwidth and stability is proposed. This drastically reduces the power dissipation for large dynamic range operation. It is also shown that adaptation does not adversely affect bandwidth or noise performance. Measured results show operation over 7 decades of current with an average power consumption of 3.45μW. The average SNR for operation at 5kHz is 65 dB.

References

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