A 2.4GHz Sub-passive RF Down-converter with Trans-frequency Current-reusing scheme achieving Low Flicker Noise and High Linearity

1st Yan Zhao
National Application Specific Integrated Circuit Center
Southeast University
Nanjing, China
zhaoy@seu.edu.cn

2nd Chao Chen
National Application Specific Integrated Circuit Center
Southeast University
Nanjing, China
c.chen@seu.edu.cn

3rd Wenjing Zhang
National Application Specific Integrated Circuit Center
Southeast University
Nanjing, China
220221700@seu.edu.cn

4th Jun Yang
National Application Specific Integrated Circuit Center
Southeast University
Nanjing, China
dragon@seu.edu.cn

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***Abstract*—This paper proposes a radio frequency (RF) down-converter, in which part of the RF transconductance (g_m) stage is reused as the bias current source of the transimpedance amplifier (TIA) to realize trans-frequency current-reusing, thereby saving 30% power consumption of the down-converter. Other from a conventional passive down-converter, TIA's DC bias current flows through the mixing switches in the proposed down-converter. Hence it is so called the sub-passive down-converter. Compared with the passive topology where flicker noise from the TIA's bias is fully fed to the intermediate frequency (IF) output, the flicker noise of the TIA's current source supplied by the RF g_m stage is up-converted and filtered out. The flicker noise corner frequency is cut-down to 20KHz, applicable for the zero-IF receiver. The linearity is also improved by the completely counteracting of third-order transconductance from PMOS and NMOS g_m transistors in the transconductance amplifier (LNTA), which is contributed by their asymmetrical bias current. Fabricated in TSMC 40nm CMOS technology, the sub-passive RF down-converter achieves 55dB conversion gain (CG) and 4dB noise figure (NF), which is suitable for high sensitivity applications. And it implements 23dBm OIP3 at 2.4GHz with 0.8mW power consumption at 0.65V supply voltage and the chip area of 0.3mm × 0.9mm.**

***Index Terms*—Direct conversion, sub-passive down-converter, transimpedance amplifier (TIA), passive down-converter, radio frequency (RF) receiver, low power, low voltage, low flicker noise, zero-IF receiver.**

I. Introduction

With the rapid growth of Internet of Things (IoT) wireless nodes, low power consumption and low cost have become the primary goals pursued by both industry and academia considering battery charging and replacement cycles [1]–[5]. With narrower intermediate frequency (IF) bandwidth and lower analog to digital converter (ADC) sampling frequency, the zero-IF receiver is more power-efficient than the low-IF receiver and relieves digital baseband (DBB) complexity and local oscillator (LO) matching requirement. However, for narrowband wireless communication standards such as Zigbee and BLE with bandwidths less than 2MHz, the low-IF receiver is preferred because the output flicker noise corner frequency is often up to 200KHz-500KHz for a typical radio frequency (RF) front-end [5]–[9]. As shown in Fig. 1(a), the passive down-converter with good linearity and noise performance of mixing switches is applicable for low-voltage designs [5], [10]. But it requires additional power dissipation of transimpedance amplifier (TIA), which is considerably high for noise and gain concerns. This paper proposes an RF down-converter, the concept is displayed in Fig. 1(b). It adopts part of the low noise transconductance amplifier's (LNTA's) PMOS transconductors to provide DC bias current for TIA, causing the linear mixer switches that flow through DC current to generate flicker noise, so it is called a sub-passive down-converter. Compared with the passive down-converter where noise from the TIA bias is fully fed to the IF output, the flicker noise of the TIA bias supplied by RF g_m stage is mixed by LO signal to be away from the IF output. With 30% power saved, the flicker noise corner frequency of the sub-passive topology is cut down to 20KHz, making it applicable for the zero-IF receiver.

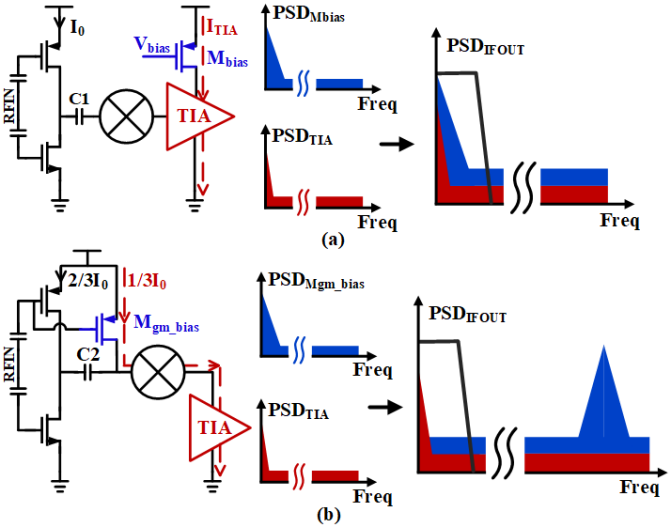

Fig. 1. Block diagrams. (a) The passive down-converter. (b) The proposed sub-passive down-converter.

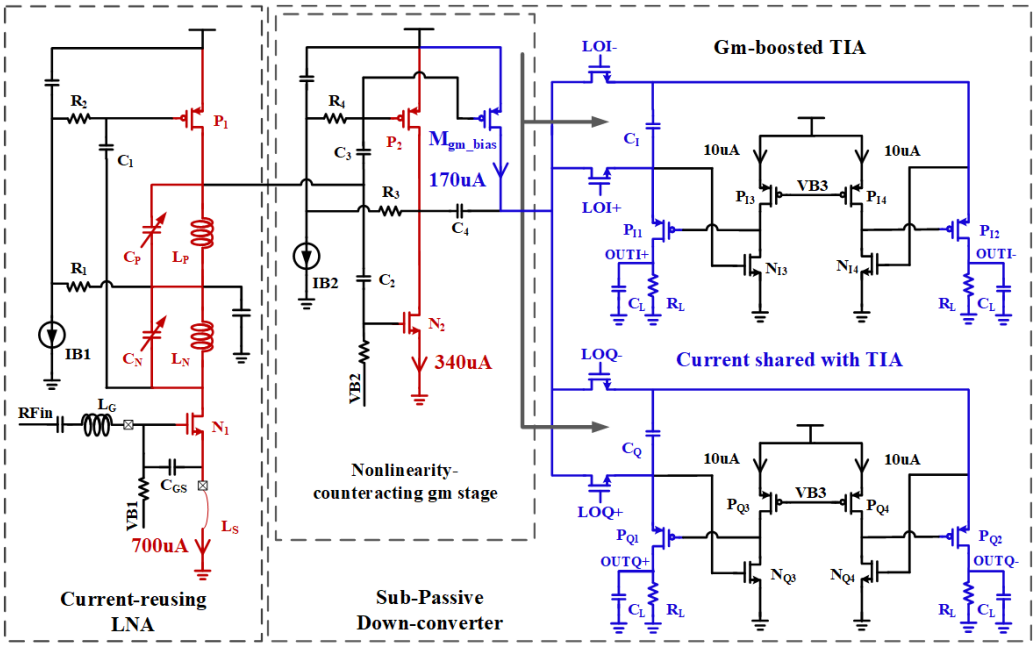

Fig. 2. The circuit schematic of the proposed sub-passive RF down-converter.

II. The Sub-passive RF Down-converter

Fig. 2 shows the proposed sub-passive RF down-converter that consists of a series feedback current-reusing low noise amplifier (LNA) and a sub-passive down-converter. The two stages of LC loaded LNA share the bias current to achieve cascaded gain without extra power consumption. The LNA realizes resistive noise-free impedance matching to obtain passive gain before active circuits for gain and noise figure improvement. In the LNTA, the PMOS transconductor M_{gm_bias} mirrors the bias current of the self-biased PMOS transconductor P2 to provide exactly replicated bias current for TIA's common-gate input transistors, eliminating the TIA's bias current source and RF coupling units to save power consumption and chip area. So M_{gm_bias} shares current with TIAs to realize RF-BB current-multiplexing and the flicker noise of M_{gm_bias} is removed at IF output, also its thermal noise is converted by mixing switches. The gm-boosted common gate TIA achieves a low input impedance as virtual ground and outputs voltage signals across the loads with first-order filtering, improving linearity.

A. Noise Analysis of the Sub-Passive Down-converter

The TIA's noise equivalent model of the sub-passive down-converter is displayed in Fig3.(a). Compared with the passive topology in Fig3.(b), DC bias current flows through the mixing switches to the TIAs along with the RF current. The slowly varying gate flicker noise of mixing switches causes a displacement in the zero-crossing point of the LO signal with the 25% duty cycle scheme. This, in turn, modulates the mixing commutation instant and generates a sequence of noise pulses, resulting in flicker noise at the output terminal. Considering the baseband component, the flicker noise current of the mixing switches is:

$$I_{e,out}(f) = \frac{2\sqrt{2}I_{DC}}{\pi V_{P,LO}} V_n(f). \tag{1}$$

Where $V_{P,LO}$ is the peak-to-peak value of the square-wave-like LO signal. In Fig.3(b), the noise current from the TIA bias transistor M_{bias} of the passive topology that fully feeds into IF output is:

$$I_{e,M_{bias}}(f) = g_{m,M_{bias}} V_n(f). \tag{2}$$

As the mixing switches turn on in the triode region, they should be strongly driven by robust LO voltage of 0.8V to maintain a low ON resistance. Therefore, the flicker noise introduced by the mixing switches of (1) is at most 1/10 that of the TIA's current source in (2). The simulated TIA's output noise of the proposed down-converter is compared with a conventional one under the same conversion gain. The sub-passive topology eliminates part of the current source, decreasing the thermal noise as illustrated in Fig. 3(c). The flicker noise of the bias current source supplied by RF g_m stage is up-converted and removed from the output signal, so the flicker noise corner frequency is cut down to 10KHz. In addition, the equivalent input noise PSD of a conventional passive down-converter and the sub-passive down-converter are demonstrated as N_p and $N_{sub,p}$ in (3) and (4), respectively.

$$N_p = \frac{2\pi^2 KT\gamma}{G_{mp}}\left(\frac{1}{4} + \frac{1}{\gamma G_{mp} R_L} + \frac{g_{mM_{bias}}}{G_{mp}} + \frac{g_{mPI3} + g_{mNI3}}{G_{mp} R_{S_M}^2 g_{mNI3}^2}\right) \tag{3}$$

$$N_{sub,p} = \frac{2\pi^2 KT\gamma}{G_{msubp}}\left(\frac{1}{4} + \frac{1}{\gamma G_{msubp} R_L} + \frac{g_{mPI3} + g_{mNI3}}{G_{msubp} R_{S_M}^2 g_{mNI3}^2}\right) \tag{4}$$

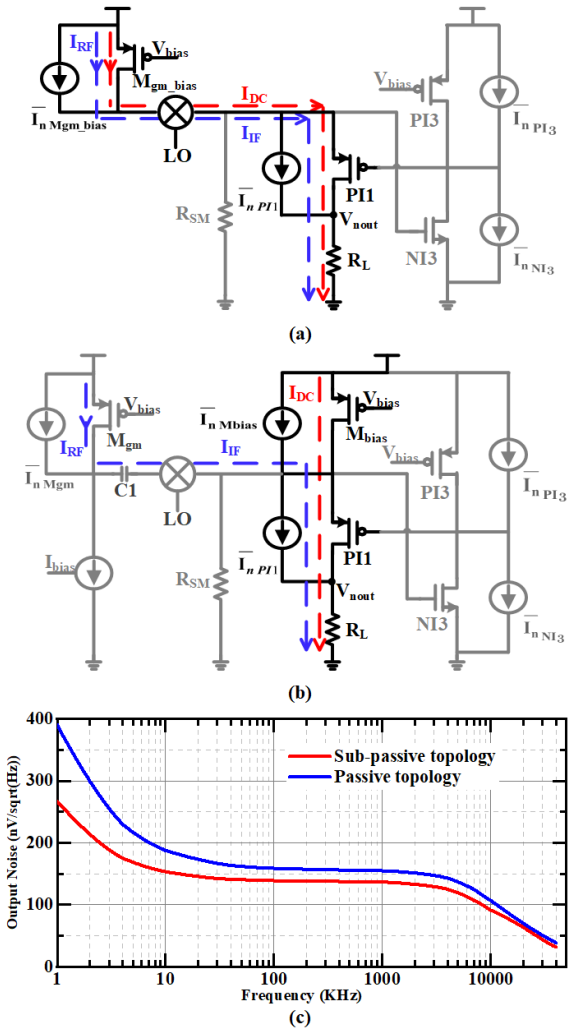

Fig. 3. The TIA's noise equivalent models of (a) the sub-passive topology; (b) the passive topology. (c) The simulated output noise.

G_{mp} and G_{msubp} represents the overall LNTA's equivalent g_m separately. It is noted that the noise of the TIA's current source in the third term of (3) is removed in (4).

B. Linearity Analysis of the Sub-Passive Down-converter

The CMOS LNTA is commonly used in low power receivers. The third-order transconductance ($g_3=\partial^3 I_{drain}/\partial V_{gs}^3$) plays a crucial role in the nonlinear distortion. As shown in Fig. 4, the g_3 curve is positive in the sub-threshold region, it increases to a peak value and then decreases, reaching zero near the threshold voltage. Subsequently, as the transistor enters the saturation region, g_3 becomes negative, gradually decreasing to a negative peak value before experiencing a rebound. The regions of positive and negative influence exerted by the g_3 exhibit bilateral symmetry along the X-axis (Vin). To fully counteract the g_3, the bias current of the PMOS transconductor should be 1.5 times stronger than that of the NMOS transconductor. As a result, in the conventional CMOS LNTA, nonlinearity

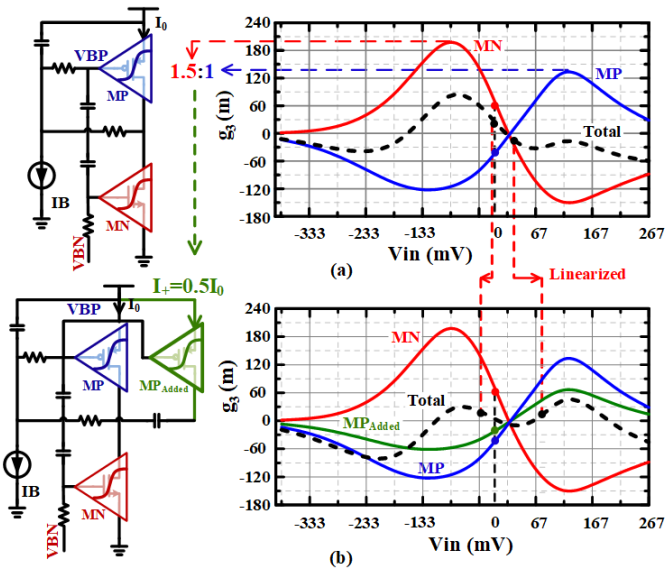

Fig. 4. Comparison of g_3 cancellation curves. (a) The CMOS LNTA topology. (b) The sub-passive topology.

cancellation can only be achieved within a narrow swing range near the bias point for input voltage. In the proposed sub-passive structure, an additional 0.5 times PMOS current provided by MP_{Added} in Fig. 4(b) makes the g_3 sum of PMOS similar to the g_3 of NMOS. Therefore, a much flatter total g_3 curve in black dash line is obtained, which indicates a much wider linear range for input voltage.

III. Measurement Results

The proposed sub-passive RF down-converter was fabricated in TSMC 40nm CMOS technology. Fig.5 illustrates the microphotography of the sub-passive down-converter and it occupies a die area of 0.3mm×0.9mm. The gate inductor and the source inductor of LNA are made off-chip to save die area. And the overall power consumption at 0.65V supply voltage is 0.8mW. By sweeping the RF input signal frequency with the LO frequency tracking, the measured results in Fig. 6(a) indicate that the peak conversion gain (CG) of 55.5dB is achieved at 2.41GHz and the CG is higher than 50dB in the frequency range of 2.40-2.48GHz. As depicted in Fig.6(b), the

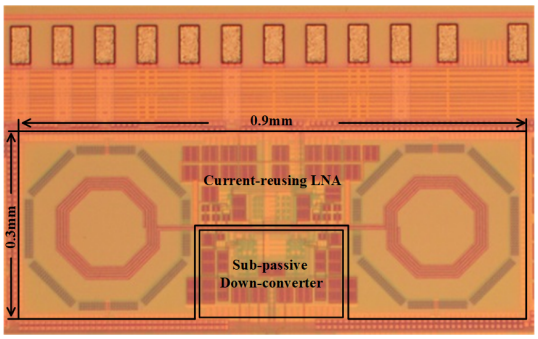

Fig. 5. Microphotography of the prototype chip.

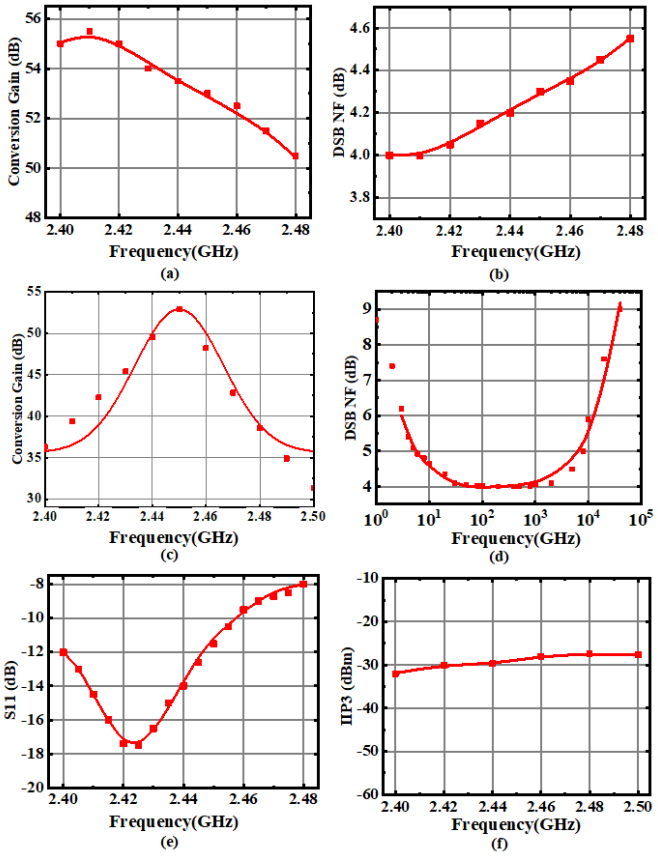

Fig. 6. The measured results of (a) conversion gain (CG) versus frequency; (b) DSB NF versus RF frequency; (c) CG at 2.45GHz LO; (d) DSB NF versus IF frequency; (e) S11 versus frequency; (f) IIP3 versus frequency.

noise figure (NF) curve exhibits an inverse trend in contrast to the CG curve, the lowest NF is 4dB at 2.41GHz and the NF is below 4.6dB up to 2.48 GHz. Fig. 6(c) presents the measured CG versus output IF frequency at 2.45GHz LO frequency, the peak CG is 53dB with 3dB bandwidth of almost 20MHz. Fig. 6(d) shows the measured DSB NF versus IF frequency at 2.4GHz LO frequency. NF remains consistently below 5dB within the IF frequency range of 10KHz to 10MHz. The flicker noise corner frequency of approximately 20KHz is done, which is applicable for zero-IF receiver in narrowband communications. The measured S11 curve in Fig. 6(e) indicates that the minimum S11 of -17.5dB is implemented at 2.42GHz, and a desirable return loss of better than 8dB is demonstrated across the entire 2.4GHz frequency band. Fig. 6(f) shows that the IIP3 is -32dBm at 5MHz and 6MHz frequency offsets from 2.4GHz, which fluctuates steadily from 2.4GHz to 2.48GHz and complies with the CG shape. The proposed down-converter compares the measured performances with the state-of-the-art works in Table I. The figure-of-merit (FoM) of 36 is implemented, showing the combined advantages of power consumption, noise, CG and IIP3.

TABLE I
COMPARISON OF STATE-OF-THE-ART WORKS

	VLSI17 [2]	*JSSC18 [3]*		*JSSC22 [4]*	*This work*
Technology	16nm FinFET	28nm		180nm	40nm
Frequency(GHz)	2.1	2.4		2.4	2.4
Supply(V)	0.4	0.18	0.3	0.8	0.65
Power(mW)	10	0.38	1.3	0.34	0.8
CG(dB)	35	34.5	41.3	57	55
DSB NF(dB)	2.5	11.3	8.8	10.5	4
IIP3(dBm)	-6*	-12.5*	4.8*	-15.5*	-32
S11(dB)	-	-10		<-20	-17.5
Area(mm^2)	0.31	1.65		0.75	0.27
FoM	27	28.8	38	39.9	36

* OOB IIP3.

$$FoM = 10log(\frac{10^{\frac{CG}{20}} \cdot 10^{\frac{IIP3-20}{20}}}{10^{\frac{NF}{20}} \cdot P})$$

IV. Conclusion

The sub-passive RF down-converter adopting the trans-frequency current-reusing scheme recycles the current of the RF transconductor to supply for the TIA, saving 30% current consumption and eliminating most of the flicker noise from the TIA. The corner frequency of flicker noise is cut down to 20KHz, making it possible to apply the zero-IF topology for narrowband communications. Furthermore, the additional PMOS transconductor in the LNTA provides a just appropriate condition to realize total counteraction for nonlinearity in a wider input voltage range, which achieves notable improvement in IIP3 at the same time. The prototype was fabricated in TSMC 40nm CMOS technology and has a chip area of 0.3mm × 0.9mm. The sub-passive down-converter implementcs a measured conversion gain of 55dB, a noise figure of 4dB and 23dBm OIP3 at 2.4 GHz with 0.8mW power consumption at 0.65V supply voltage.

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