A Low-Power Multimode Eight-Channel AFE for dToF LiDAR

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***Abstract*—This paper presents a low-power multimode eight-channel analog front-end (AFE) circuit for direct time-of-flight (dToF) LiDAR applications. The proposed AFE features rich programmability in: a) Two operation modes, parallel mode and selectable mode to save power; b) Two coupling modes, anode and cathode coupling with photodiodes (PDs); c) Two gain modes, high-gain mode for PIN-PD and low-gain mode for APD. Correspondingly, several circuit design techniques have been proposed to support the programmability including: a) Reconfigurable TIA with awake/sleep state and high/low gain mode switching; b) Symmetrical pulse width control to match the pulse width of anode and cathode coupling and input over load protection; 3) Glitch reduction for channel switchover in selectable mode. Designed in 0.18-µm CMOS technology, the AFE achieves bandwidth of 180 MHz, transimpedance gain of 100 dBΩ, input-referred noise current of 2.1 pA/$\sqrt{\text{Hz}}$ and output swing of 1 $V_{\text{pp,diff}}$. The channel switchover time is around 10 ns in selectable mode. The channel power consumption is 50 mW in parallel mode and 11.4 mW in selectable mode.**

***Index Terms*—dToF LiDAR, AFE circuit, multi-channel, low-power, multimode.**

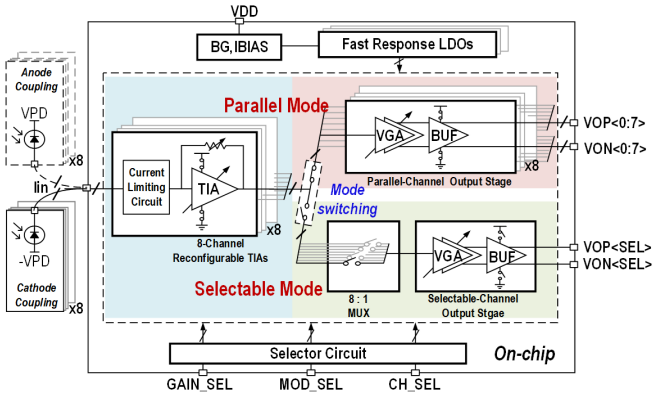


Fig. 1. System architecture of the proposed AFE circuit.

I. Introduction

Recently, direct time-of-flight (dToF) is currently the mainstream technology for automotive LiDAR system. It offers detailed, quantifiable 3D sensing with a longer detection range and faster measurement capabilities [1] - [3]. In the receive end, a single-channel receiver is usually insufficient in meeting the demands in real-time response and rapid imaging, multi-channel receiver is usually employed [2] - [6], which is able to provide more comprehensive and accurate environment perception capabilities.

Conventional LiDAR receivers are mostly designed for a fixed application scenario [5], with predetermined detection distance, scanning speed, and sensing device. However, the rapid development as well as enriched application scenarios of LiDAR demand more versatile sensing device, which is able to reconfigure itself based on the actual condition.

First, for long range detection, the Avalanche Photodiodes (APDs) is often employed to provide high gain, which require high bias voltages as high as 100 V. On the other hand, Positive-Intrinsic-Negative Photodiodes (PIN-PDs), while offering smaller gain that may still justify its use in short range detection, can operate at much lower power supply voltages of a few volts. The analog front-end (AFE) circuit needs to offer different gain modes to cater APD or PIN-PD with low noise and sufficient bandwidth. Moreover, based on the type of PD, both anode and cathode coupling between the PD and AFE need to be supported. The AFE is expected to handle both positive and negative current pulse with symmetrical response, allowing a unified backend processing scheme. Last, depending on the system topology, the LiDAR may need to either simultaneously feed all channel outputs to a multichannel backend in a high-speed multi-line scanning mode, or sequentially output multi-channel signal to a single-channel backend in a moderate speed rotational scanning mode which may allow low power operation.

Based on these considerations, this work proposes a low-power multimode eight-channel AFE circuit, as illustrated in Fig. 1. The signal path consists of 8 reconfigurable TIAs, 8 parallel-channel output stage and a selectable-channel output stage. In parallel mode, the TIAs are routed with the 8 parallel-channel output stage, constituting a high-speed 8 channel AFE. In selectable mode, the TIAs feed to the selectable-channel output stage one by one, allowing temporary turned off of the 7 inactive TIAs, and complete turned off of the 8 parallel-channel output stage, which can dramatically reduce power by roughly a factor of 8 in the signal path. The TIA provides two gain modes tailored to APD and PIN-PD, respectively. The symmetrical pulse width control is designed to handle input current of both polarities, and obtain symmetrical output response. Additionally, fast response low-dropout regulators (LDOs) are integrated to generate a 1.8 V power supply for each channel, facilitating rapid establishment during channel switching in this chip. The rest of the papers details the circuit design techniques to support such a versatile AFE.

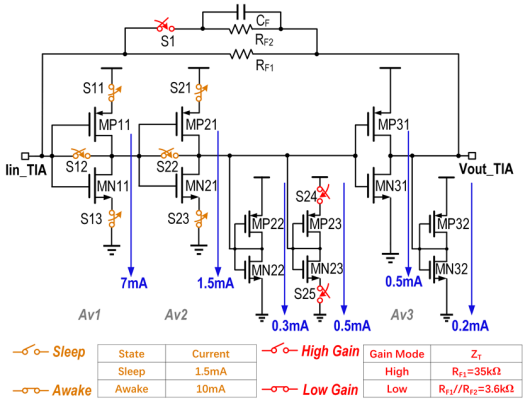


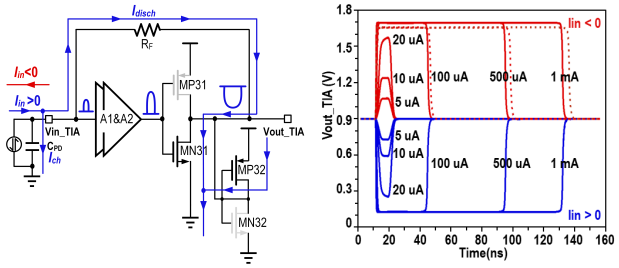
Fig. 2. Schematic of the proposed reconfigurable TIA.

II. Circuit Design

A. Reconfigurable TIA

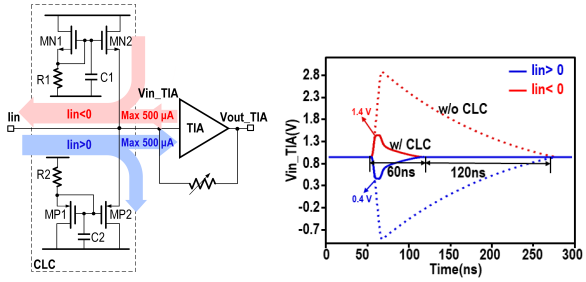
Implemented in the shunt feedback topology, the forward amplifier of TIA adopts a self-biased gm-gm inverter structure. The gain design of each stage follows the optimal noise theory [7]. The proposed reconfigurable TIA has two gain modes, as shown in Fig. 2. The high-gain mode of the TIA is set as 91 dBΩ, such a vast gain for the better noise performance, and that of low-gain is 73.6 dBΩ. The switches, marked in red color, are used to reconfigure the gain mode. For high gain mode, R_{F1} is selected as the feedback resistor and S24/S25 are turned off, leaving a single load stage in the second stage amplifier to increase the forward gain and match R_{F1}. In low gain mode, R_{F2} and R_{F1} in parallel serve as the feedback resistor, together with the frequency compensation capacitor C_{F}. Additionally, S24/S25 are turned on to bring in MP23/MN23 to decrease the open-loop gain of the forward amplifier and to ensure stability.

TIAs are designed to be able to be switched off when needed to reduce power consumption. Simply cutting off the power supply of TIAs will disrupt their DC operating points, resulting in excessive recovery time. To solve that, a sleep-state DC-maintaining TIA topology is proposed. The switches, highlighted in orange in Fig. 2, enable the topology switching between awake and sleep state. As for wake state, S11/S13/S21/S23 are turned on while S12/S22 are turned off. Concurrently, the proposed TIA delivers sufficient gain and bandwidth for input current signal amplification. During sleep state, S11/S13/S21/S23 are off, while S12/S22 are on. The forward amplifier then essentially consists of only the third stage powered on in the signal path to sustain the DC status, which will shorten the power-on time of the other two forward amplifiers. The quick TIA awake/sleep will not only save power, but also accelerate channel switching. In selectable mode in eight TIAs, only one is awake while others are asleep, then the current consumption is 10 mA + 1.5 mA × 7 = 20.5 mA instead of 10 mA × 8 = 80 mA in parallel mode, a 4x reduction.



(a) (b)

Fig. 3. (a) Large signal response. (b) Transient response of $V_{\mathrm{out\_TIA}}$ before (dashed lines) and after (solid lines) optimization with different input current in high gain mode.



(a) (b)

Fig. 4. (a) Schematic of CLC. (b) Transient response of $V_{\mathrm{out\_TIA}}$ without (dashed lines) and with (solid lines) CLC in 2mA current in high gain mode.

B. Symmetrical pulse width Control

The proposed AFE supports both anode and cathode coupling with PD, which is reflected in its capability to handle input current of both direction. We define the current flowing into the TIA as positive, denoted as $I_{\mathrm{in}} > 0$, shown in blue in Fig. 3(a) and the current flowing out of the TIA as negative, represented by $I_{\mathrm{in}} < 0$, shown in red. However, the polarity shift in input and output nodes of the proposed TIA shows a dynamic effect and asymmetry pulse width occurs under these two polarities. When $I_{\mathrm{in}} > 0$, a portion of the input current (I_{disch}) flows through RF while the rest (I_{ch}) charges the parasitic capacitance of PD. If I_{in} is large, the signal $V_{\mathrm{out\_TIA}}$ features a negative polarity, resulting in the shutdown of MP31 and MN32, and the discharge current that flows through R_{F} is the difference of that in MN31 and MP32. In large signal mode, the discharge current not only determines the output amplitude, but also the expansion time of the output pulse. Therefore, the aspect ratio of MP32 and MN32 are optimized in this design so that the discharge current of both directions equal. Fig. 3(b) shows the improved results with different input current. It shows a symmetric pulse width regardless of the current direction, which supports a flexible design and unified backend processing in both polarities.

In addition, a current limiting circuit (CLC) is added for over-current protection, as shown in Fig. 4. MP2 or MN2 is on when the signal $V_{\mathrm{in\_TIA}}$ is larger than 1.4 V or lower than 0.4 V which is determined by R1 and R2 in two conditions, respectively. C1 and C2 are filtering capacitors [8]. In that case, maximum 500 μA level of the input current flows through

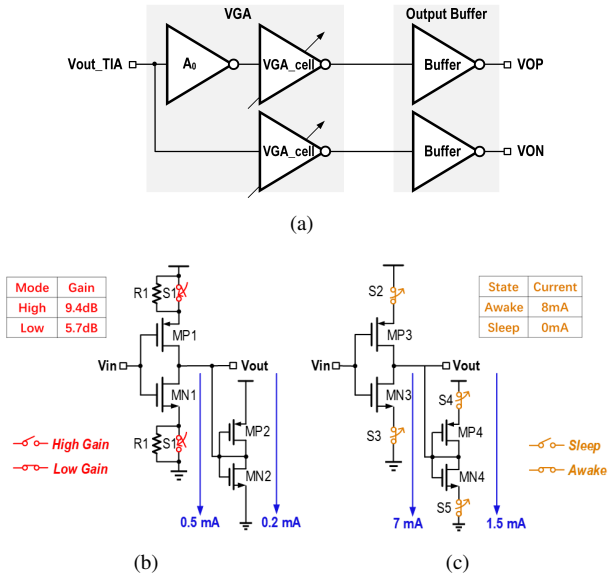


Fig. 5. Schematic of (a) the proposed output stage, (b) VGA_cell, (c) buffer.

the TIA while the rest is absorbed by the CLC to protect the input. Further, pulse width under high current is also limited, which will allow a faster operation cycle. Otherwise, two consecutive received pulse will overlap under high refreshing rate and cause obscure.

C. Output stage

The output voltage of the TIA should be further amplified for subsequent circuit measurement. So the output stage including an output buffer which improves the driving capability is shown in Fig. 5(a). Since a high R_{F} is chosen in the TIA to optimize the noise behavior, a variable gain amplifier (VGA) with a source negative feedback resistor R_1 is used here to adjust the overall circuit gain, as depicted in red in Fig. 5(b). In high gain mode, R_1 is paralleled and the gain of this stage is then decreased from 9.4 dB to 5.7 dB without additional increase in power consumption. An amplifier A_0 with unity gain is set here so that this stage converts the single-ended signal from TIA into an equivalent differential signal and transmit it to the buffer. The schematic of the proposed output buffer is shown in Fig. 5(c). The 50-Ω output buffer provides an output swing of 1 $V_{\mathrm{pp,diff}}$ while only consuming 16 mA, which is smaller than that realized in a CML of at least 20 mA. Similarly to the reconfigurable TIA, the buffer can also switch between awake and sleep state to save power. Referring to Fig. 1 again, in the selectable mode, only the buffer in selectable-channel is awake while other buffers in parallel-channel are asleep, which achieves a power reduction of 8x in the buffer parts.

D. Glitch Reduction

In selectable mode, maximum low power is achieved by turning off unused TIA channels. When TIA in CHm is set in awake state, its output is routed to the selectable-channel output stage, while other TIAs are in sleep state, as shown

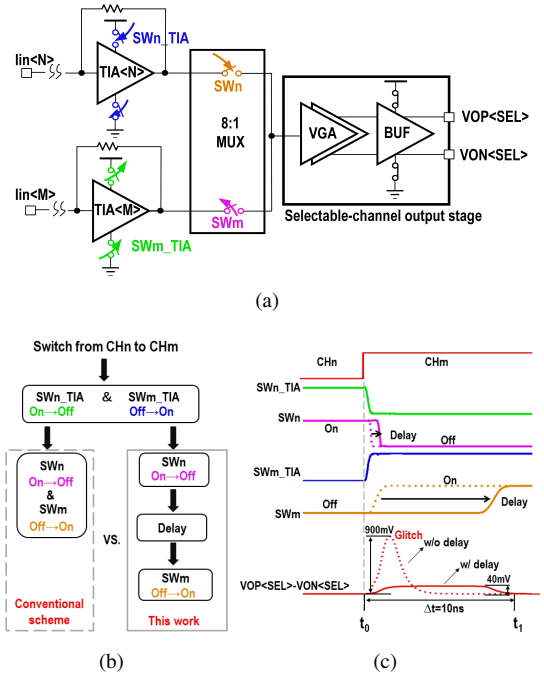


Fig. 6. (a) The topology for switching from CHn to CHm in selectable mode. (b) Illustration of the conventional scheme and our work. (c) Channel switching time w/ (solid lines) and w/o (dashed lines) delay.

in Fig. 6(a). However, these switching activities will generate glitches at the output, which may cause misjudgment in the subsequent circuit. Thus, it is important to minimize the amplitude of the glitch as much as possible, and the timing of the switching activity is optimized in Fig. 6(b). The SWn and SWm are extended for a period of time before off or on, instead of changing simultaneously. Meanwhile, SWm connects later than SWm_TIA, preventing the glitch of the immediate reconfiguration of TIA. In this way, the amplitude of the glitch is reduced. The channel switching time (Δt) is defined as the existence time of the output glitch [5]. As a result, it only takes 10 ns for the system to settle shown in Fig. 6(c).

III. Post-Layout Simulation Results

The layout of the proposed eight-channel AFE circuit, with an area of 1 mm × 5 mm, is shown in Fig. 7. Each channel is designed with its own power and ground supply to minimize crosstalk. All post-layout simulations are based on 50-Ω output loading and the input with a parasitic capacitance of 3 pF. The parasitic inductance and resistance of the power supply, ground, input and output bonding wires are also considered.

Fig. 8 shows the simulated transient pulse response, where the input current of eight channel varies from 5 μA to 2 mA. In parallel mode, all the output voltage waveform shows little distortion and good symmetry. The maximum output swing is up to 1 $V_{\mathrm{pp,diff}}$. In the selectable mode, CH0 to CH7 are sequentially selected and the outputs and inputs are mapped on by one. The channel switchover time is around 10 ns.

Fig. 9 presents the frequency response of two gain modes. The maximum gain is 100 dBΩ and the bandwidth is 180

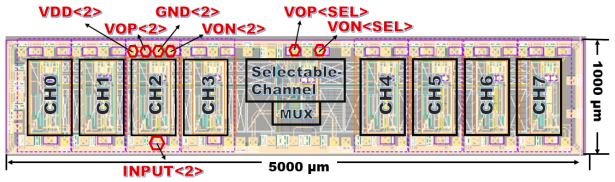
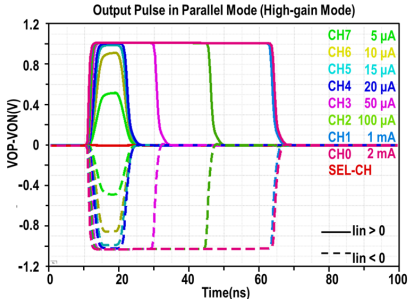
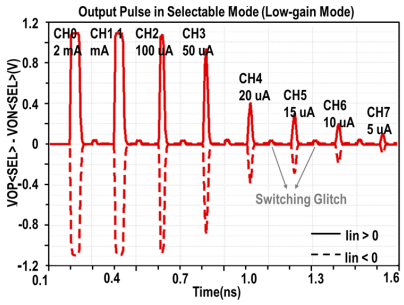


Fig. 7. Chip layout of the proposed AFE circuit.



(a)



(b)

Fig. 8. Simulated pulse response for each channel with various I_{in} in (a) parallel mode with high-gain, (b) selectable mode with low-gain.

MHz. The average input-referred noise current is 2.1 $\text{pA}/\sqrt{\text{Hz}}$ and 3.3 $\text{pA}/\sqrt{\text{Hz}}$ in high and low gain mode, respectively.

Fig. 10 illustrates the power consumption distribution for each mode. Due to the buffer in parallel channel and the unselected TIA channels are in a sleep state while VGAs are always awake, it can be seen that switching from parallel mode to selectable mode reduces the power consumption of the output stage and TIAs, enabling total power reduction by nearly 4x.

Finally, Table I summarizes the main performances of the proposed AFE and comparison with recent published works. Our work shows overall good performance in noise, gain and output swing. Due to the selectable mode, the power consumption is much smaller. The offer of both parallel and selectable modes, and the capability of both anode and cathode coupling makes itself more flexible to applications.

IV. Conclusion

This paper presents a low-power multimode eight-channel AFE circuit for dToF LiDAR applications. Designed in 0.18-μm CMOS, this chip is equipped with both parallel mode and selectable mode, which can achieve high echo detection capability in both rotational scanning and multi-line scanning. The power consumption is also dramatically reduced in selectable mode thanks to awake/sleep of many circuit blocks. In addition, it not only offers the compatibility with bot anode and cathode coupling with PD, but also delivers symmetrical output response. In summary, this work shows a good performance and provides a versatile solution for dToF LiDAR application of various applications.

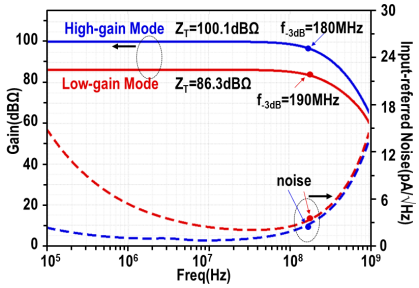


Fig. 9. Post-layout simulation of the frequency response of the AFE.

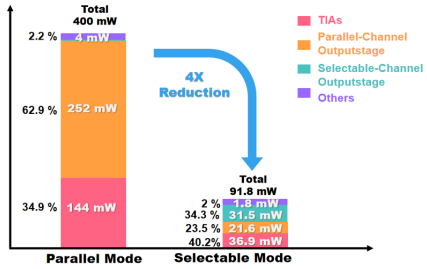


Fig. 10. Power consumption of each module in two operation modes.

TABLE I
Performance Summary And Comparison

		[1] TCAS2-2023	[2] Sensor-2023	[3] VLSI-2020	[4] TCAS1-2022	This work#
Technology		180-nm CMOS	180-nm CMOS	180-nm CMOS	65-nm COMS	**180-nm COMS**
No. of Channel		1	5	8	8	**8**
Function Features		Single-channel	Parallel-channel only	Parallel-channel only	Selectable-channel only	**Parallel and Selectable channels**
PD	CPD(pF)	1.5	0.49	2.0	1.0	**3.0**
	Coupling Type	Anode coupling	Anode coupling	Anode coupling	Cathode coupling	**Anode and Cathode coupling**
Gain(dBΩ)		100	87	101	106	**100**
Bandwidth(MHz)		260	577	190	220	**180**
Noise(pA/√Hz)		3.3	15.4	3.74	5.1	**2.1**
Output Swing($V_{pp,diff}$)		1	0.58*	1	-	**1**
Area(mm^2)		0.89	2.2	2.54	1.44	**5**
Channel Switchover (ns)		-	-	-	15*Δ	**10**
Core power consumption /Ch(mW)		153	50.6	45	-	**49.3** (In parallel mode)
			-	-	17	**10.5** (In selectable mode)

Simulation Results. * Read from figure.
ΔDefined as the exisiting time of switching time in [5].

Acknowledgment

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