A Mixed-Signal TIA with Input Restoring ADC

David-Peter Wiens, Björn Driemeyer, and Maurits Ortmanns
Institute of Microelectronics, University of Ulm,
Albert-Einstein-Allee 43, Ulm, Germany, david-peter.wiens@uni-ulm.de

2024 IEEE International Symposium on Circuits and Systems (ISCAS) | 979-8-3503-3099-1/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISCAS58744.2024.10557979

***Abstract*—Transimpedance amplifiers (TIAs) are used in a wide variety of low noise current sensing frontends. A recently proposed mixed-signal TIA (MS-TIA) is an extension of the integrator-differentiator TIA but including digitization and digital differentiation. However, the MS-TIA requires a high resolution analog-to-digital converter (ADC) in order to maintain good sensitivity. Capacitive digital-to-analog converter (C-DAC) based successive approximation register (SAR) ADCs achieve high resolution at medium bandwidth with good power efficiency, however require a power hungry ADC input driver. In this paper, a combination of the MS-TIA and a modified C-DAC reset scheme is presented, which eliminates the need for a high performance ADC input driver, resulting in major improvements regarding power consumption and linearity. The results are verified by transistor level simulations in a standard 180nm CMOS technology.**

***Index Terms*—current sensing, low noise, MS-TIA, C-DAC, SAR ADC**

I. Introduction

Low noise and wideband current sensing frontends are needed in numerous bio- and chemical sensors. For example in DNA sequencing current-based biosensors are used, achieving a $\sim\mathrm{fA}/\sqrt{\mathrm{Hz}}$ noise floor, with a concurrent $\sim$MHz bandwidth (BW) [1], [2].

The integrator-differentiator TIA (I-D-TIA) has received attention to realize such low noise current sensing frontends, cf. Fig. 1a [3]–[5]. Notably the operational amplifier (OA) used to realize the analog differentiator dominates the power consumption in low noise, wideband I-D-TIAs, due to its high demands in gain and unity gain bandwidth product (GBW) [5].

Recently, a mixed-signal TIA (MS-TIA) was introduced in [6], where the power hungry analog differentiator is replaced by an analog-to-digital converter (ADC) with subsequent digital differentiation, cf. Fig. 1b. It was shown that it can achieve improved power efficiency and implicit digitization when compared to an all analog I-D-TIA. In the MS-TIA, other than in current-mode delta-sigma modulators (CM-DSMs) [7]–[10], the feedback loop only counteracts the DC input current to avoid saturation of the integrator. However the MS-TIA requires an ADC with higher resolution, compared to an ADC needed in a comparable I-D-TIA [6]. Thus, a high power efficiency of the ADC inside the MS-TIA is crucial.

In recent years, capacitive digital-to-analog converter (C-DAC) based successive approximation register (SAR) ADCs have been shown to achieve tremendously good power efficiency, achieving high resolution and BW in the MHz range [11]–[13]. Such ADCs can be used in MS-TIAs [6]. However, the input buffer of the ADC can easily consume the same or even much more power than the ADC itself [12], [13].

In this paper, a modified reset scheme for C-DAC based SAR ADCs is presented in combination with the MS-TIAs,

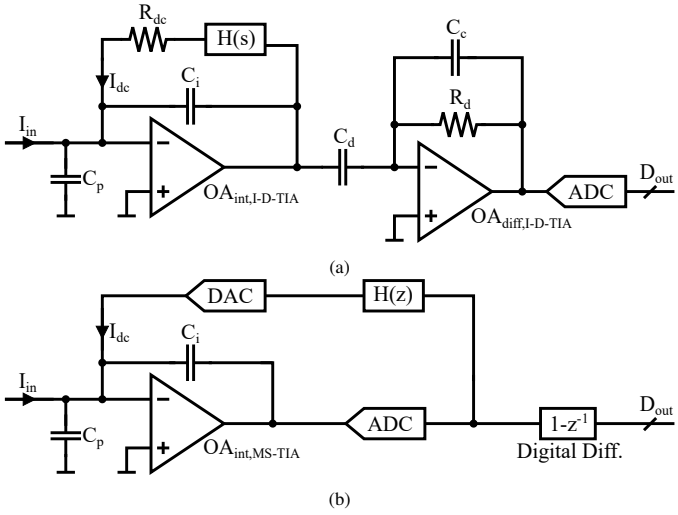

Fig. 1: (a) I-D-TIA [3] and (b) MS-TIA [6].

which removes the power hungry buffer. This is achieved by exploiting the lowpass transfer characteristic of the input integrator and by reconstructing the charge on the sampling capacitor of the previous sampling point, referred to as input restoring (IR) reset scheme.

The paper is organized as follows: Sec. II reviews the working principle of the MS-TIA and Sec. III introduces the idea of the IR reset scheme. Sec. IV shows design considerations and models for the MS-TIA utilizing a IR SAR ADC. Sec. V presents transistor level simulation results and Sec. VI concludes the work.

II. Mixed-Signal TIA

The MS-TIA, cf. Fig. 1b, was introduced in [6] as an alternative topology to the I-D-TIA in order to: 1) move the differentiation from the analog into the digital domain, removing the power hungry analog differentiator; 2) have a direct digitizing sensor readout; 3) benefit from scaled technologies; 4) have implicitly the possibility to implement a mixed-signal DC servo loop [2], [10]. For readability of this paper, some important properties of the MS-TIA are shortly reviewed. The input referred noise power spectral density (PSD) of the MS-TIA, neglecting the ADC and sampling, is given by [6]

$$I_{\mathrm{n,in}}^2 \approx I_{\mathrm{n,DAC}}^2 + \omega^2 C_i^2 \left(1 + \frac{C_p}{C_i}\right)^2 V_{\mathrm{n,OA}}^2, \qquad (1)$$

where C_i is the integrator capacitor, C_p the parasitic input capacitor, $V_{\mathrm{n,OA}}$ the integrator OA voltage noise and $I_{\mathrm{n,DAC}}$ the DC servo loop DAC current noise. Due to the highpass

shaping, the integrator OA noise dominates the total integrated noise in wideband MS-TIAs. Thus, by neglecting the noise from the DC servo loop, the total integrated noise of the MS-TIA is found by integration over the signal BW $0 \ldots f_{\max}$

$$I^2_{\text{rms,in}} \approx 4\pi^2 \frac{f^3_{\max}}{3} C_i^2 \left(1 + \frac{C_p}{C_i}\right)^2 V^2_{\text{n,OA}}. \quad (2)$$

The required resolution of the ADC used inside the MS-TIA is defined by the noise power at the output of the integrator due to its OA noise, which is given by [6]

$$V^2_{\text{rms,int}} = \frac{\pi}{4} f_{\max} \left(1 + \frac{C_p}{C_i}\right)^2 V^2_{\text{n,OA}}. \quad (3)$$

The maximum BW $f_{\max}$ of the MS-TIA is defined by the $\text{GBW}_{\text{OA,int}}$ of the OA used for the integrator [6]

$$\text{GBW}_{\text{OA,int}} = \left(1 + \frac{C_p}{C_i}\right) f_{\max}. \quad (4)$$

It was then shown in [6] that the ADC in a MS-TIA requires less oversampling when compared to an ADC subsequent to the I-D-TIA in order to avoid noise-folding by aliasing; but it was also shown that the ADC in a MS-TIA requires significantly more signal-to-noise ratio (SNR) as its (white) quantization and thermal noise is highpass filtered by the digital differentiator and is thus significantly increased towards the bandwidth edge. With an design example, [6] could show that state-of-the-art (SoA) ADCs with Schreier figure of merit (FoM_{Sch}) $\geq$173 dB could fulfill this requirement, and the overall MS-TIA would then consume less power when compared to the analog differentiator implementation of the I-D-TIA.

III. Proposed Modified Reset Scheme

SoA C-DAC based SAR ADCs achieve signal-to-noise-and-distortion ratio (SNDR) >90 dB at BWs in the MHz range, while reaching FoM_{Sch} above 180 dB [11]–[14].

Often disregarded, the input buffer of such high-performance ADCs will increase the power consumption significantly, as it needs to handle rail-to-rail signals and drive sampling capacitors in the range of tens of pF (due to kT/C noise), while the settling time is only a fraction of the sampling frequency, thus a few ns long. Therefore, the ADC input buffer can easily dominate the power consumption of the whole ADC, reducing the FoM_{Sch} by 3-6dB in [12], [13].

Advantageously, in the case of the MS-TIA the input of the ADC is the output of the integrator, cf. Fig. 1b, which has a lowpass transfer characteristic. Thus, assuming a full scale (FS) input change of the ADC at Nyquist-rate is far too pessimistic. For a maximum inband sinusoidal input signal $I_{\text{in}}(t) = I_{\max} \sin(2\pi f_{\text{in}} t)$ the maximum input signal change of the ADC, from one sampling point nT_S to the next $(n+1)T_S$, is given by

$$\begin{aligned} \Delta V_{\text{ADC,max}} &= \int_{nT_S}^{(n+1)T_S} \frac{1}{C_i} I_{\max} \underbrace{\sin(2\pi f_{\text{in}} \tau)}_{\leq 1} d\tau \quad (5) \\ &\leq \int_{nT_S}^{nT_S+1} \frac{I_{\max}}{C_i} d\tau = \frac{I_{\max}}{C_i} T_S, \end{aligned}$$

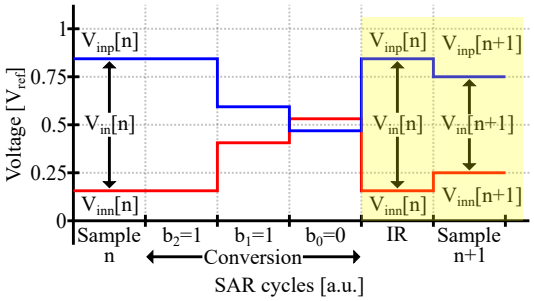

Fig. 2: Exemplary IR in an 3-bit merged-capacitor switching scheme followed by a restoring phase for the original input voltages (highlighted in yellow).

where T_S is the sampling period and C_i the integrator capacitor. Eq. (5) shows that the maximum input change of the ADC is dependent on the sampling period T_S, the maximum input current $I_{\max}$ and the integrator capacitor C_i. In low noise and wideband MS-TIA the sampling period T_S is small, also for the targeted sensing application, the maximum inband signal $I_{\max}$ is small. Moreover, the integrator capacitor C_i is not arbitrarily small, due the required dynamic range (DR) of low frequency inband signals [5]. Thus the maximum change $\Delta V_{\text{ADC,max}}$ is expected to be much smaller than the FS of the integrator output.

By reconstructing the charge distribution on the sampling capacitor, such that the input sample is restored after a SAR conversion cycle, the ADC buffer only has to deliver the difference in sampling charge between consecutive samples, which is the core idea of the charge restoring switching scheme applied to the ADC in the MS-TIA: Using a C-DAC based SAR ADC, the input is sampled on the C-DAC, then the SAR algorithm approximates the input sample by redistributing the charge on the C-DAC. By now re-flipping the switches in the C-DAC to the initial sampling position without tying the sampling capacitors to a fixed reference, the charge on the capacitors is redistributed such that the original input sample is restored. This concept is referred to as *IR SAR ADC*. Then, the ADC input buffer has to deliver only the sampling charge equivalent to the voltage difference of the next sample, illustrated in Fig. 2.

IV. System Model

In order to verify the effectiveness of the proposed IR SAR ADC used in combination with the MS-TIA, an exemplary MS-TIA is designed partly using VerilogA modeling and transistor level design in a standard 180 nm technology. As design example for noise and DR, the SoA I-D-TIA implementation from [5] was chosen, with important specifications summarized in Tab. I. The MS-TIA is thereby designed as fully-differential (FD) circuit to match the reference ADCs in [11]–[13]; further, also recent CM-DSMs were implemented as FD circuits [9], [10].

A. MS-TIA: Integrator transistor level design

A FD two-stage Miller compensated OA with class-A output stage has been designed on transistor level in a 180 nm technology. In order to keep the integrator gain comparable to the single-ended implemented I-D-TIA [5], an integrator capacitor

parameter	value	comment
f_{min}	100 Hz	minimum signal BW
f_{max}	7.7 MHz	maximum signal BW
V_{DD}	1.8 V	supply voltage
C_i	220 fF	integrator feedback cap
C_p	3.08 pF	tot. parasitic input cap
C_d	20 pF	differentiator input cap
R_d	470 kΩ	differentiator feedback resistor
R_{dc}	1 GΩ	DC servo loop resistor
$R_{\text{I-D-TIA}}$	153 dB	tot. transimpedance
I_{max}	±21 nA	max. input current
$I_{\text{rms,in}}$	440 pA_{rms}	total input referred noise
$V_{\text{n,OA}}$	1.72 $\text{nV}/\sqrt{\text{Hz}}$	int. OA noise, using Eq. (2)

TABLE I: I-D-TIA specifications from [5].

of $C_i = 110\,\text{fF}$ is used for the FD integrator. Using Eq. (4) and $C_i = 110\,\text{fF}$ the OA requires a GBW of 223 MHz. The output of the OA is periodically loaded by the sampling capacitor $C_S = 8.1\,\text{pF}$ of the coarse SAR ADC stage. The required current in the integrator OA is defined by the demanded GBW, load capacitor C_S, and voltage noise, see Tab. I. In total the integrator OA requires a bias current of 900 µA from a 1.8 V supply and achieves a phase margin of 78°.

In the design considerations of the integrator OA a possible limitation due to slew rate (SR) is not considered. However since the integrator is driving the large sampling capacitor C_S of the ADC, SR should not be neglected. Thus, class-AB stages would be more practical. However a simple OA design was chosen, as it does not compromise the statements about the advantages of the IR reset scheme.

For simplicity and also because it has no implication on the proposed IR reset scheme, an analog DC servo loop was implemented using ideal components, while guidelines for transistor-level design of the DC servo loop can be found numerously [3], [5], [15].

B. MS-TIA: ADC design

A 16 bit two-step SAR ADC has been implemented using VerilogA models and ideal components, cf. Fig. 3, based on the designs from [11], [12]. IR was implemented in the first stage of the two-step SAR ADC by removing the reset switches of the C-DAC.

Using Eq. (3) and the parameters from Tab. I, with $C_i = 110\,\text{fF}$, the noise power in the MS-TIA at the output of the integrator is calculated, resulting in an rms-noise of $V_{\text{rms,int}} = 123\,\mu\text{V}$. An ADC adding the same amount of integrated inband noise, assuming a FD rail-to-rail input swing, requires a $\text{SNR}_{\text{MS-TIA}} = 80\,\text{dB}$. A SNR of 86 dB, i.e. 1 bit more, is chosen for the ADC, in order to not significantly influence the total inband noise [6].

The quantization of the two-step SAR ADC is then split into two parts: first a 7 bit C-DAC based SAR ADC is used for the coarse quantization, then a 9 bit ADC is used for the fine quantization. An inter-stage gain of 128 is chosen for the residual amplifier (RA). Dither is added inside the fine quantizer to achieve a SNR of 86 dB. The kT/C-noise limited sampling capacitance of the coarse stage is $C_S = 8.1\,\text{pF}$, with a unit capacitor of 63.3 fF. A merged capacitor switching scheme is implemented for the coarse SAR ADC [16].

The two-step SAR ADC is operating at a Nyquist-rate of 15.4MS/s. Following [6], using no oversampling and 1 bit more resolution in the ADC, leads to a x2 increase in total input referred noise in the MS-TIA. Even though an increase of oversampling ratio (OSR) to ∼4 would make the aliased noise negligible [6], a value of OSR = 1 is nevertheless chosen, as it does not only reduce ADC complexity, but is also the worst-case scenario for the proposed IR reset scheme, since for higher sampling rate (thus smaller T_S) the maximum input change of the ADC decreases, see Eq. (5).

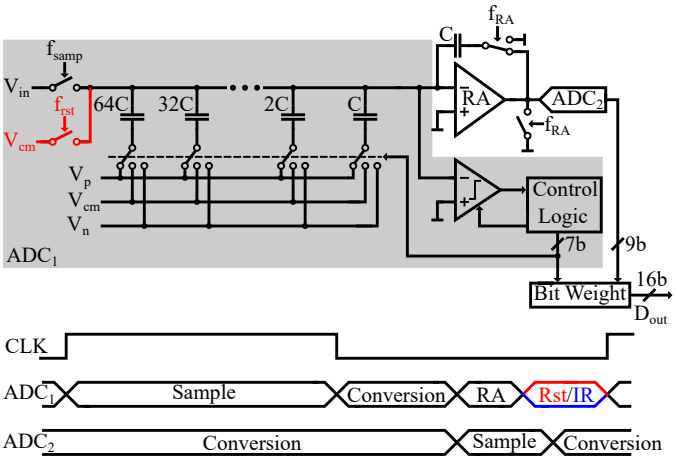

Fig. 3: Two-step SAR ADC and timing diagram. The conventional SAR ADC is marked in red, the IR SAR is marked in blue.

Using Eq. (5) and Tab. I, this results in a maximum integrator output change between consecutive samples of only 6.2 mV. Therefore, the integrator only has to provide a fraction of the sampling charge, when using the proposed IR SAR ADC, compared to a conventional SAR ADC with periodically reset sampling capacitor: a sampling capacitor being reset to $V_{CM} = 0.9V$ and then facing a FS integrator output would need rail-to-rail charging by about $\pm 900mV$, which is about 150 times larger than the expected worst-case charging of $\pm 6.2mV$ when avoiding the reset by IR switching. Moreover, with the smaller input voltage step and a constant sampling time, the required absolute settling accuracy can be achieved with larger time constant, which all together translate to relaxed sampling switch on-resistance, as well as smaller GBW and SR of the OA within the integrator of the MS-TIA.

V. Simulation Results

Transient simulations were performed using Spectre circuit simulator. Fig. 4 shows the input referred noise PSD, 1) of the MS-TIA without the influence of sampling and quantization by choosing very high sampling frequency and no quantization before differentiation (indicated as *reference*), 2) of the MS-TIA combined with a conventional SAR ADC, 3) of the MS-TIA combined with the proposed IR SAR ADC, and 4) of the MS-TIA combined with the conventional SAR ADC but with an ideal ADC input buffer. It can be seen that the three MS-TIAs with ADC achieve approximately the same noise performance. Compared to the reference spectrum, the input referred noise PSD of all MS-TIAs increases by a factor of 2, which is due to noise aliasing by sampling at Nyquist-rate, as already derived in [6] and discussed above.

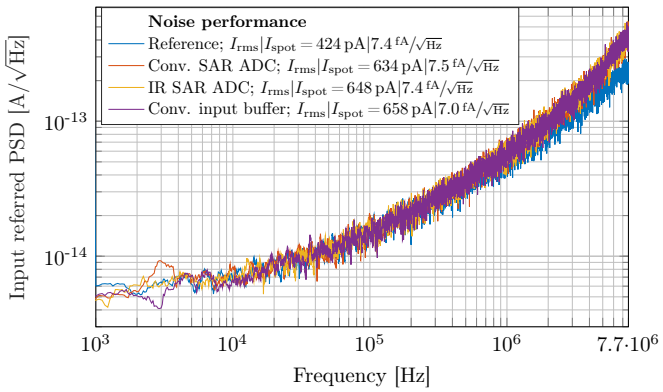

Fig. 4: Input referred noise PSD of different MS-TIAs, with total integrated noise I_{rms} and minimum spot-noise I_{spot} given.

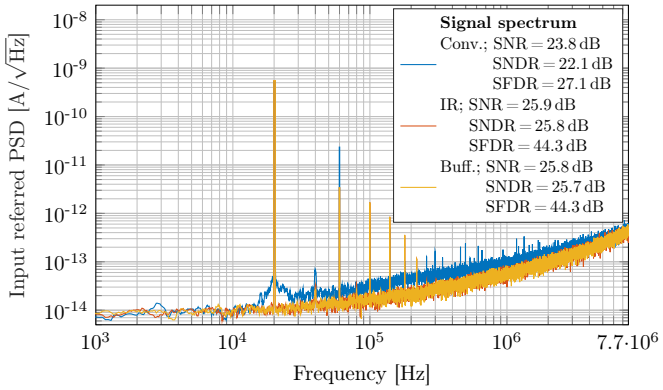

Fig. 5: Input referred PSD (2^{18}-point FFT) with deep inband input sinusoidal of the MS-TIA with different ADC topologies.

Fig. 5 shows the input referred PSD of the three MS-TIAs with low frequency (20 kHz) input sinusoidal. The input signal has an amplitude of 18 nA, which - according to Tab. I - is close the the maximum specified input signal. At this input sinusoidal frequency and magnitude, the swing at the output of the integrator is −3 dBFS. Assuming a total input referred noise of 650 pA_{rms}, see Fig. 4, an ideal SNR of 26 dB is achieved. Please note that also SoA low noise and wideband I-D-TIAs achieve similar DR, which is due to the high gain and highpass shaped integrator OA noise [3]–[5], and it is often the spot noise which is of interest.

Notably, the MS-TIA with IR SAR ADC achieves a more than 3 dB higher SNDR and more than 17 dB better spurious-free dynamic range (SFDR), compared to the MS-TIA with conventional SAR ADC. Further, there is no significant difference in the spectrum of the MS-TIA using the proposed IR SAR ADC compared to the MS-TIA using a conventional SAR ADC but employing an ideal ADC input buffer.

Fig. 6 shows the total harmonic distortion (THD) versus the input amplitude of the three different MS-TIAs. An input sinusoidal of 20 kHz was chosen. The MS-TIA with IR SAR ADC shows up to 15 dB better THD at large input amplitudes when compared to the MS-TIA with conventional SAR ADC. Also, almost no difference in THD is observable between the MS-TIA with the proposed IR SAR ADC and a MS-TIA using a conventional SAR ADC but employing an ideal ADC input buffer; hence, the remaining THD of the MS-TIA with IR SAR ADC is only caused by the limited output range of the integrator OA, and not by the sampling onto the C-DAC. Thus, it can be concluded that the proposed IR reset scheme renders a dedicated ADC input buffer obsolete and the integrator can fulfill the purpose of driving the ADC sampling capacitor.

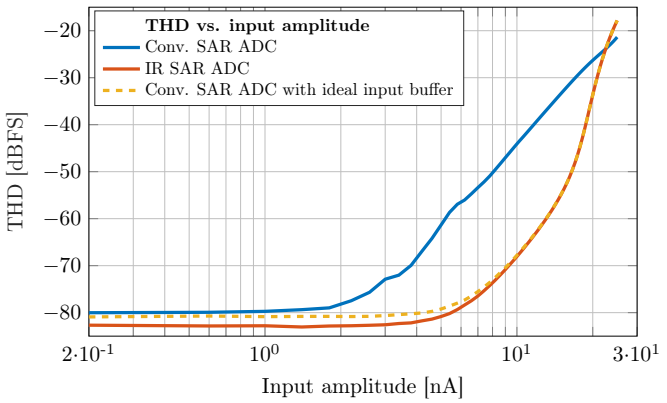

Fig. 6: THD versus input amplitude of the MS-TIAs with different ADC topologies. THD saturates for small input signals due to finite noise power at the location of the HDs.

VI. Conclusion

A modified reset scheme was presented for C-DAC based SAR ADCs employed in a MS-TIA, which allows to drastically decrease the ADC buffer requirements. By removing the reset phase of the C-DAC in a conventional SAR ADC, the charge on the sampling capacitors is redistributed, such that the original input sample is restored. Thus, the ADC driver only has to provide the difference in charge between consecutive samples. This is highly advantageous with the recently proposed MS-TIAs, since the integrator output is changing slowly with respect to the sampling rate.

By using an IR SAR ADC in a MS-TIA, compared to a conventional SAR ADC, the SNDR is improved by 3 dB, with a more than 20 dB better linearity over a wide input range. Also, the MS-TIA with IR SAR ADC achieves the same linearity performance compared to a MS-TIA using a conventional SAR ADC but employing an ideal ADC input buffer. Consequently, a power hungry rail-to-rail ADC buffer can be omitted in a MS-TIA, when the IR reset scheme is applied, which highly improves the power efficiency of the MS-TIA.

Acknowledgment

This work was funded by the German Federal Ministry of Education and Research through the Project VE-FIDES under Grant 16ME0258.

REFERENCES

[1] M. Crescentini, M. Bennati, M. Carminati, and M. Tartagni, "Noise Limits of CMOS Current Interfaces for Biosensors: A Review," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, no. 2, pp. 278–292, Apr. 2014.

[2] C.-L. Hsu, H. Jiang, A. G. Venkatesh, and D. A. Hall, "A Hybrid Semi-Digital Transimpedance Amplifier With Noise Cancellation Technique for Nanopore-Based DNA Sequencing," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 9, no. 5, pp. 652–661, Oct. 2015.

[3] G. Ferrari, F. Gozzini, A. Molari, and M. Sampietro, "Transimpedance Amplifier for High Sensitivity Current Measurements on Nanodevices," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1609–1616, May 2009.

[4] M. Taherzadeh-Sani, S. M. Hussain Hussaini, H. Rezaee-Dehsorkh, F. Nabki, and M. Sawan, "A 170-dBΩ CMOS TIA With 52-pA Input-Referred Noise and 1-MHz Bandwidth for Very Low Current Sensing," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 5, pp. 1756–1766, May 2017.

[5] M. Häberle, D. Djekic, D. Krüger, M. Rajabzadeh, M. Ortmanns, and J. Anders, "An Integrator-Differentiator Transimpedance Amplifier Using Tunable Linearized High-Value Multi-Element Pseudo-Resistors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 8, pp. 3150–3163, Aug. 2022.

[6] D.-P. Wiens, M. Sporer, B. Driemeyer, and M. Ortmanns, "A Mixed-Signal Integrator-Differentiator-TIA," *IEEE Transactions on Circuits and Systems II: Express Briefs (Early Access)*, pp. 1–1, 2023.

[7] M. Amayreh, Y. Manoli, and M. Keller, "A 1.85 fA/$\sqrt{}$Hz Fully Integrated Read-out Interface for Sub-pA Current Sensing Applications," in *IEEE 43rd European Solid State Circuits Conference (ESSCIRC)*, Sep. 2017, pp. 356–359.

[8] M. Rajabzadeh, M. Häberle, A. Jain, and M. Ortmanns, "An Integrated Readout for Current Sensing based on a $\Sigma\Delta$ Modulator with Switched Capacitor Feedback," in *IEEE 45th European Solid State Circuits Conference (ESSCIRC)*, Sep. 2019, pp. 321–324.

[9] S.-H. Wu, Y.-S. Shu, A. Y.-C. Chiou, W.-H. Huang, Z.-X. Chen, and H.-Y. Hsieh, "9.1 A Current-Sensing Front-End Realized by A Continuous-Time Incremental ADC with 12b SAR Quantizer and Reset-Then-Open Resistive DAC Achieving 140dB DR and 8ppm INL at 4kS/s," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, Feb. 2020, pp. 154–156.

[10] T. Seol, S. Lee, G. Kim, S. Kim, E. Kim, S. Baik, J. Kung, J.-W. Choi, A. K. George, and J. Lee, "A 1V 136.6dB-DR 4kHz-BW $\Delta\Sigma$ Current-to-Digital Converter with a Truncation-Noise-Shaped Baseline-Servo-Loop in 0.18μm CMOS," in *2023 IEEE International Solid- State Circuits Conference (ISSCC)*, Feb. 2023, pp. 482–484.

[11] A. ElShater, P. K. Venkatachala, C. Y. Lee, J. Muhlestein, S. Leuenberger, K. Sobue, K. Hamashita, and U.-K. Moon, "A 10-mW 16-b 15-MS/s Two-Step SAR ADC With 95-dB DR Using Dual-Deadzone Ring Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3410–3420, Dec. 2019.

[12] M. Li, C. Y. Lee, A. ElShater, Y. Miyahara, K. Sobue, K. Tomioka, and U.-K. Moon, "10.4 A Rail-to-Rail 12MS 91.3dB SNDR 94.1dB DR Two-Step SAR ADC with Integrated Input Buffer Using Predictive Level-Shifting," in *2023 IEEE International Solid- State Circuits Conference (ISSCC)*, Feb. 2023, pp. 1–3.

[13] Y. Guo, J. Jin, X. Liu, and J. Zhou, "A 60-MS/s 5-MHz BW Noise-Shaping SAR ADC With Integrated Input Buffer Achieving 84.2-dB SNDR and 97.3-dB SFDR Using Dynamic Level-Shifting and ISI-Error Correction," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 2, pp. 474–485, Feb. 2023.

[14] B. Murmann, "ADC Performance Survey 1997-2023," [Online]. Available: https://github.com/bmurmann/ADC-survey.

[15] J.-H. Noh, "Frequency-Response Analysis and Design Rules for Capacitive Feedback Transimpedance Amplifier," *IEEE Transactions on Instrumentation and Measurement*, vol. 69, no. 12, pp. 9408–9416, Dec. 2020.

[16] V. Hariprasath, J. Guerber, S.-H. Lee, and U.-K. Moon, "Merged Capacitor Switching Based SAR ADC with Highest Switching Energy-Efficiency," *Electronics Letters*, vol. 46, no. 9, p. 620, 2010.