Analog Test Bus Structure for Wide-Bandwidth High-Frequency Measurements

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***Abstract*—Analog test buses facilitate the testing of analog components in integrated circuits through dedicated test ports and switches. IEEE 1149.4 is an analog test bus standard that can be calibrated with simple gain correction but cannot calibrate for other sources of error present at higher frequencies, leading to inaccurate measurements. This paper presents a novel analog test bus structure with greater calibration capabilities inspired by the vector network analyzer (VNA) calibration approach that uses multiple known calibration references. These references were integrated within the test bus constructed of voltage and current buffers. IEEE 1149.4 and the proposed test bus were first compared via simulation and then through a discrete component PCB implementation, both aimed at measuring a transimpedance amplifier (TIA). The simulation showed that the proposed test bus exactly measured the amplifier with little error while 1149.4 deviated at higher frequencies. These results were echoed in the physical experiment, with the proposed 4-port deviating slightly from the ideal due to the mismatch inherent in the PCB experiment.**

***Index Terms*—calibration, S-parameter, VNA, analog test bus, current buffer, voltage buffer, error correction, BIST**

I. Introduction

Testing the analog components of an integrated circuit is costly and time consuming. This is especially true for components that operate in the RF and millimeter wave (mmWave) frequency range. Existing testing strategies include either external equipment that has limited visibility into the circuit or Built-In Self-Test (BIST) and Design-for-Test (DfT) strategies that are application-dependent and have trade-offs in chip area and reliability. These strategies aim to verify basic functionality, characterize performance, or locate defects.

An alternative approach is an analog test bus, which has the advantage of accessing many internal components through dedicated test ports and general switching circuitry. IEEE 1149.4 [1] is the established analog test bus standard. Fig. 1 shows 1149.4 configured to test an internal device under test (DUT). A major limitation of 1149.4 is the maximum operating frequency, which has prevented its use in RF or mmWave applications [2]. 1149.4 implementations usually have a large series resistance and shunt capacitance from the switches and bus size, limiting the bandwidth [3]–[5]. In [3], an implementation of 1149.4 was proposed using analog buffers that slightly improved the measurement frequency to 30 MHz. All current 1149.4 circuits aimed at RF applications are essentially BIST approaches using application-specific circuits to perform the RF functions, and use 1149.4 to relay information at DC or low frequency [6]–[9].

The established way to measure high-frequency analog components is by using high-quality external test equipment such as a vector network analyzer (VNA) [10], [11]. A VNA can accurately measure high-frequency signals due to its calibration procedure, which accounts for errors in the probe cable, probe contact, and measurement setup. Knowing these systematic errors, the true DUT can be de-embedded from the DUT measurement. Fig. 2 shows the typical VNA setup with the calibration measurements.

Combining the high-frequency measurement capabilities and calibration methodology of a VNA with the benefits of an on-chip analog test bus would allow the VNA to seamlessly switch between measuring calibration references and DUTs connected to the test bus from one set of test bus pins. The VNA calibration can be adapted to include the systematic errors that the test bus adds. This paper proposes a novel buffer-based analog test bus structure that uniquely applies a calibration methodology to de-embed the effects of the test bus's active and passive components to extend measurement bandwidth. A discrete component PCB implementation was built to compare the 1149.4 and proposed test buses.

The remainder of this paper is organized as follows. Section II presents the proposed analog test bus and main structural differences compared to 1149.4. Section III covers the calibration procedure. Section IV provides details on the simulation and PCB implementation. Section V presents the results of the simulation and PCB experiment. Section VI concludes the paper and discusses future work.

II. Proposed Analog Test Bus

The high-level structure of the proposed 4-port analog test bus is shown in Fig. 3. It features aspects of the 1149.4 test bus and the typical VNA calibration setup. The backbone of the 4-port test bus is voltage and current buffers capable of being turned on/off to act as switches and route signals to/from circuits connected to the test bus.

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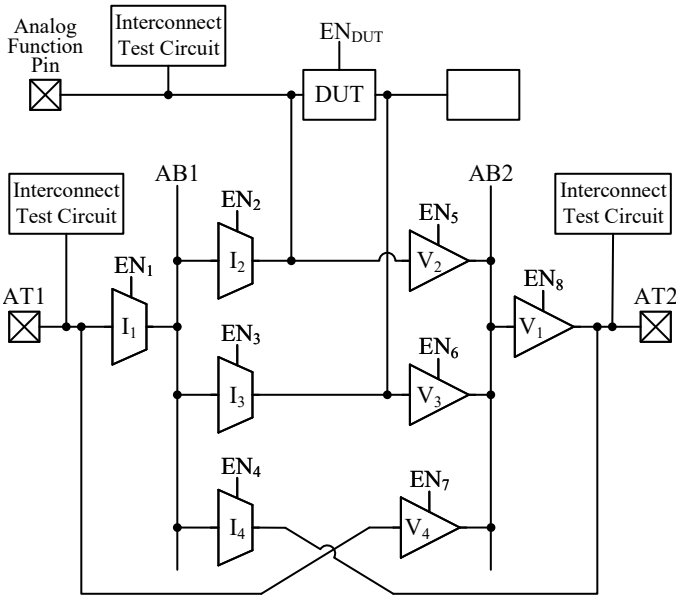

Fig. 1. IEEE 1149.4 analog test bus structure with voltage and current buffers for internal DUT [1].

The switching buffers allow the system to move between three distinct operation modes: mission, test, and calibration. Mission mode is the default state when the DUT operates normally and the entire test bus is disabled. Test mode uses the VNA and the first buffer group to measure the DUT. Calibration mode uses the three other buffer groups separately to measure the calibration references (Cal1 - 3).

The four test ports (AT1 - 4) are each connected to an internal test bus (AB1 - 4) that is then connected to the buffers. AT1 and AT2 are input ports that connect to the test signal source and current buffers to drive the signal to the DUT or calibration references. AT3 and AT4 are output ports that connect to the voltage buffers to relay the test signal off-chip. Near the test ports are the Interconnect Test Circuit blocks which would perform basic port connection testing as in 1149.4, although they are not used during test bus measurements. Transmission lines between the test ports and buffers represent parasitic elements from long traces/interconnects that are accounted for during calibration.

Compared to 1149.4, the proposed test bus has fewer buffers in the signal path and two additional test ports. These additional test ports facilitate a more extensive and accurate calibration approach that accounts for errors in buffer gain, input/output impedance, and long traces/interconnects. 1149.4 calibration paths (I_4 and V_4) only measure the gain of the current and voltage buffers.

III. Calibration

Calibration aims to characterize all systematic errors in the test bus structure and correct the DUT measurement. To accomplish this, a VNA-style calibration procedure determines the systematic errors using known reference circuits built into the test bus.

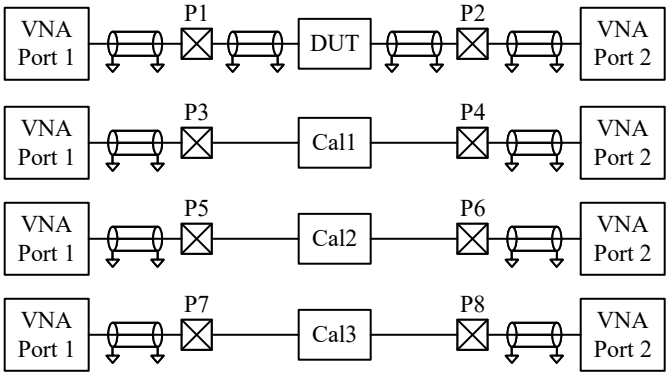

Fig. 2. Typical VNA measurement setup with calibration.

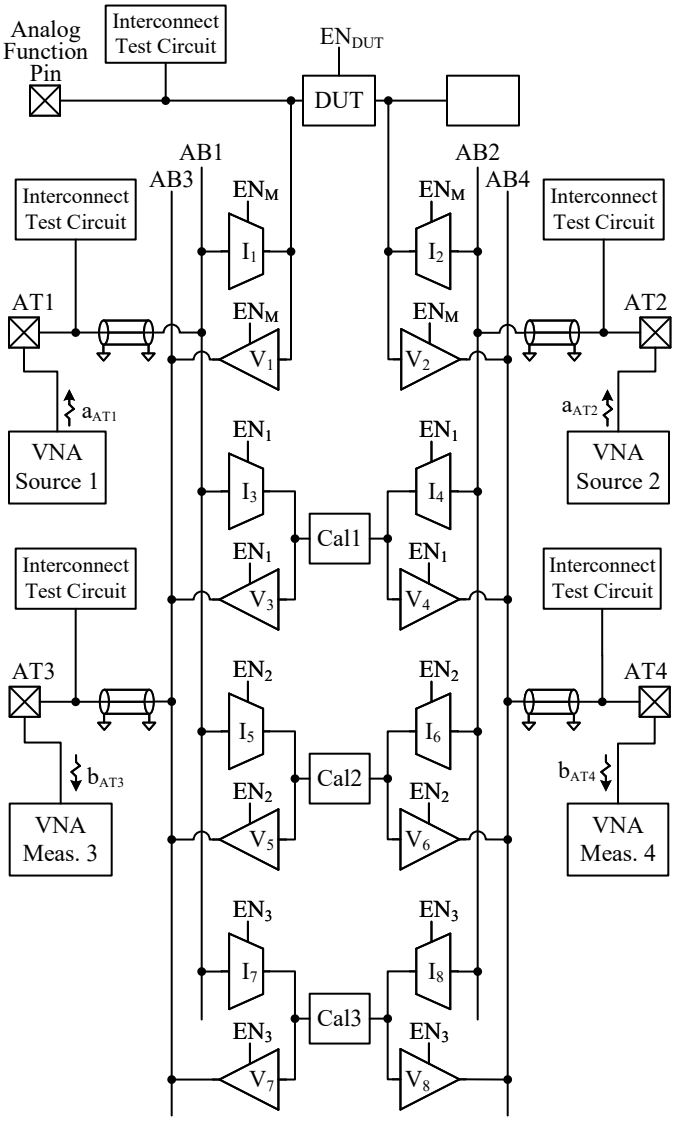

Fig. 3. Proposed 4-port analog test bus.

A. 2-Port Calibration Model Background

The calibration problem can be modeled as a cascade of 2-port network blocks, as seen in Fig. 4. The A_{dut} 2-port net-

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work, for example, represents all circuitry from the test ports to the edge of the DUT, including cables, probes, parasitic elements, transmission lines, and current/voltage buffers.

The calibration algorithm works under the assumption that the 2-port networks $A = A_{dut} = A_{cal1} = A_{cal2} = A_{cal3}$ and $B = B_{dut} = B_{cal1} = B_{cal2} = B_{cal3}$. The physically different components that make up these 2-port networks must therefore be matched as closely as possible. Otherwise, the calculated A_{dut} and B_{dut} will be less accurate. This problem also exists in normal VNA measurement setups because the VNA probes must be moved between the calibration standards and the DUT. This movement causes inconsistencies in probe placement and cable parasitics that are a known major contributor to measurement error [10], [12]. In the proposed analog test bus, the VNA probes and cables stay static as the buffers change.

Solving for the error parameters in the A and B 2-port networks is done by constructing a system of equations from the three calibration paths in Fig. 4

$$\mathbf{T_{M1}} = \mathbf{T_A}\mathbf{T_{cal1}}\mathbf{T_B} \tag{1}$$

$$\mathbf{T_{M2}} = \mathbf{T_A}\mathbf{T_{cal2}}\mathbf{T_B} \tag{2}$$

$$\mathbf{T_{M3}} = \mathbf{T_A}\mathbf{T_{cal3}}\mathbf{T_B} \tag{3}$$

where $\mathbf{T_{M1-3}}$ are the measured calibration path T-parameters, $\mathbf{T_A}$ is the input error T-parameters, $\mathbf{T_B}$ is the output error T-parameters, and $\mathbf{T_{Cal1-3}}$ are the known calibration reference T-parameters. Solving the system of equations for $\mathbf{T_A}$ and $\mathbf{T_B}$ completes the DUT measurement equation

$$\mathbf{T_{M0}} = \mathbf{T_A}\mathbf{T_{DUT}}\mathbf{T_B} \tag{4}$$

where $\mathbf{T_{M0}}$ is the measured DUT path T-parameters which can then be rearranged to solve for the DUT

$$\mathbf{T_{DUT}} = \mathbf{T_A^{-1}}\mathbf{T_{M0}}\mathbf{T_B^{-1}}. \tag{5}$$

This type of calibration and error de-embedding is well established in the VNA calibration literature and is also known as the 8-term error model [10], [13]. The exact approaches to solving for the error terms can vary and depend on the types of calibration references used. This paper used the approach presented in [14] and [15].

B. 4-Port Test Bus to 2-Port Conversion

The proposed 4-port test bus is mapped to the 2-port calibration model by only using the measured VNA S-parameters from one port to another according to

$$\mathbf{S_{M0-3}} = \begin{bmatrix} \frac{b_1}{a_1} & \frac{b_1}{a_4} \\ \frac{b_4}{a_1} & \frac{b_4}{a_4} \end{bmatrix} = \begin{bmatrix} \frac{b_{AT3}}{a_{AT1}} & \frac{b_{AT3}}{a_{AT2}} \\ \frac{b_{AT4}}{a_{AT1}} & \frac{b_{AT4}}{a_{AT2}} \end{bmatrix} \tag{6}$$

where $\mathbf{S_{M0-3}}$ are the measured S-parameters, a_{1-4} and b_{1-4} are the waves noted in Fig. 4, and a_{AT1-2} and b_{AT3-4} are the waves noted in Fig. 3.

Converting the measured $\mathbf{S_{M0-3}}$ to $\mathbf{T_{M0-3}}$ is done by

$$\mathbf{T_{M0-3}} = f(\mathbf{S_{M0-3}}). \tag{7}$$

where f is the matrix transformation function [16].

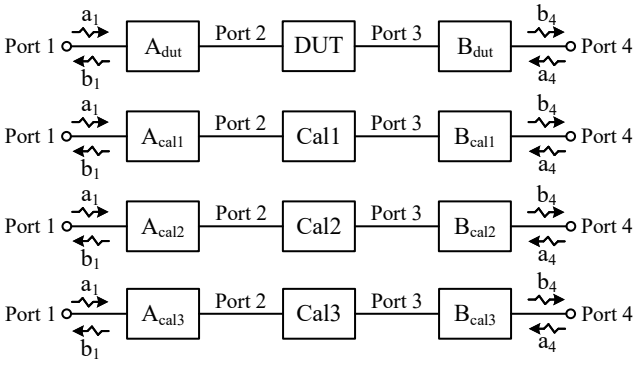

Fig. 4. 2-port network calibration model.

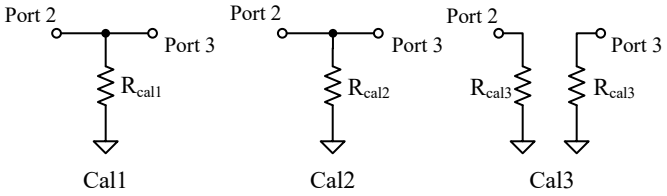

Fig. 5. Calibration references integrated within the proposed test bus.

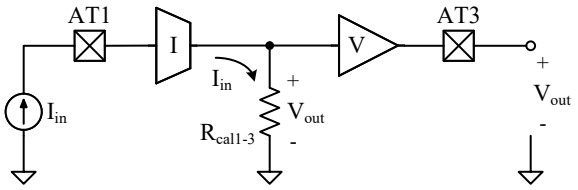

Fig. 6. R_{cal1-3} low-frequency measurement setup equivalent circuit.

C. Calibration References

VNA calibration can use many types and arrangements of calibration references. Most references are built on a standalone substrate and are based on static physical structures such as ideal loads, shorts, or transmission lines [10]. The 4-port test bus requires references that can be integrated along with the test bus buffers.

Load resistors to ground are used as the 4-port test bus calibration references, as shown in Fig. 5. The first two standards are through-type standards, and the third is a reflect-type standard similar to that of the common through-reflect-line (TRL) used for VNAs [12], [17]. The value of R_{cal1-3} need not be known beforehand and can be measured with a low-frequency test signal assuming that the voltage and current buffers are ideal at low frequencies, as shown in Fig. 6.

IV. Design of Experiment

The proposed analog test bus's use case is integrated within a chip like 1149.4. To first test the high-level topology and calibration methodology, a discrete component implementation assembled on a PCB was constructed. Both 1149.4 and the proposed analog test bus were built using the same components to compare their relative performance.

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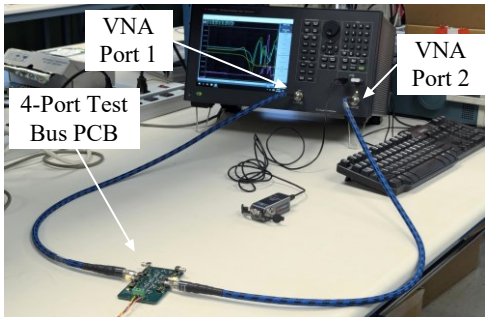

Fig. 7. Photo of VNA test setup measuring the proposed 4-port test bus.

The Texas Instruments OPA861 transconductance amplifier was used as a voltage or current buffer and the Texas Instruments LMH6609 Op-Amp was used as a transimpedance amplifier DUT. Both test buses were first simulated using PSPICE models provided by Texas Instruments for the OPA861 and LMH6609. To switch on/off components, discrete DIP switches were inserted into the power lines to cut power to the components. The Interconnect Test Circuit block was not built because it is irrelevant to test bus measurements of a DUT. A Keysight E5063A ENA Vector Network Analyzer performed the S-parameter measurements. A photo of the bench test setup is shown in Fig. 7. An additional copy of the DUT was built unconnected to any test bus to provide a directly measured reference transimpedance.

V. Results

Fig. 8 shows the results of the SPICE simulation. The proposed test bus tracked the reference DUT transimpedance exactly across all frequencies, while the 1149.4 measured transimpedance peaks higher and rolls off earlier. This error in the 1149.4 result is likely due to loading effects and resonance between the buffers and DUT not captured during the simple 1149.4 calibration. For example, the calibration current buffer with an ideal zero-impedance load performs differently from the current buffer loaded by the DUT.

Fig. 9 shows the PCB experimental result of both test buses and generally follows what was seen during the simulations. 1149.4 starts deviating at 30 MHz while the 4-port test bus tracks the reference DUT measurement from DC to 150 MHz. Above 150 MHz the 4-port test bus predicts additional resonating not seen in the reference DUT measurement. This difference could be explained by mismatches in the calibration paths or DUTs. As discussed in Section III, mismatches between buffers will cause errors in the final results, and these mismatches are amplified at high frequencies. Additionally, there could be mismatches between the reference DUT and test bus DUT in performance or parasitic elements. This mismatch would mean that the reference DUT and 4-port test bus results would not be expected to match, especially at high frequencies.

As indicated by the simulations, when the 4-port test bus has ideal buffer matching and is compared to an ideal reference DUT measurement, it can exactly de-embed the transimpedance. Implementing the 4-port test bus with discrete

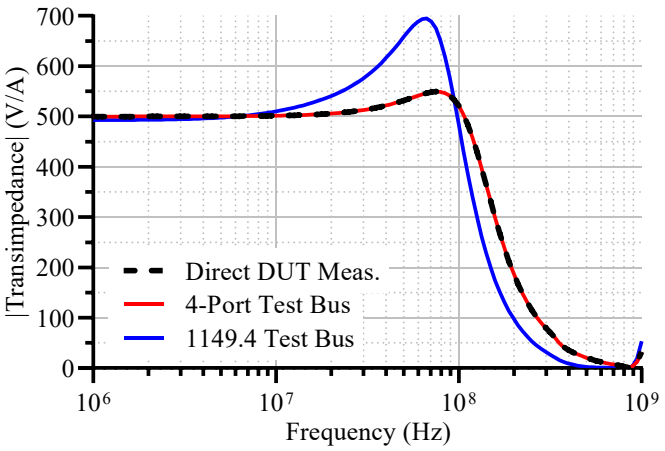

Fig. 8. Simulation results comparing the transimpedance measured from the proposed 4-port and 1149.4 test bus to a direct measurement of the DUT.

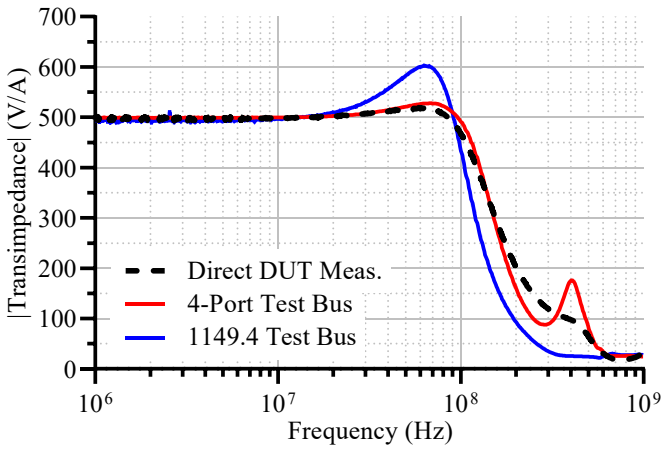

Fig. 9. Experimental results comparing the proposed 4-port and 1149.4 test bus to a direct measurement of the DUT.

components raises the challenge of closely matching the measurement paths and obtaining a reference DUT measurement that mirrors what the test bus sees. These issues and an overall bandwidth limitation due to PCB parasitic elements are inherent in a PCB implementation. Integrating the 4-port test bus on-chip would improve the matching between the buffers and extend the measurement bandwidth.

VI. Conclusion

This paper proposed a novel analog test bus topology with VNA-style calibration abilities which improved on the existing analog test bus standard by increasing the maximum possible test frequency. Compared to 1149.4, more error sources can be accounted for and de-embedded from the DUT measurement. Results from both a simulation and PCB implementation showed that the proposed test bus followed the expected transimpedance closely while 1149.4 overshot the calibration at the edge of the amplifier's bandwidth. Future work includes testing the 4-port test bus with different test targets and integrating the 4-port test bus onto a test chip.

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