A Low-Power Wireless Optical SoC for Fluorescence Monitoring

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2025 IEEE International Symposium on Circuits and Systems (ISCAS) | 979-8-3503-5683-0/25/$31.00 ©2025 IEEE | DOI: 10.1109/ISCAS56072.2025.11044147

***Abstract*— This paper presents a low-power, optical system-on-chip (SoC) enabling wireless fluorescence detection. The proposed SoC, in size of 2 × 2.7 mm², integrates a high-sensitivity optical front-end, battery management unit and energy harvesting, and a wireless data transceiver. A fast-settling transimpedance amplifier (TIA) ensures rapid startup and minimizes power consumption, supported by dual-mode low dropout regulators (LDO regulators) for efficient power management. The SoC achieves ultra-low power, 1 µW, operation with 0.5 pA sensitivity, suitable for non-invasive cellular monitoring. The SoC is implemented using 65 nm CMOS technology.**

Keywords*— *Implantable SoC, Low-Power Design, Wireless Optical Sensor, Fluorescence detection

I. Introduction

Fluorescence detection at the cellular level is essential for studying various biological processes both in vivo and in vitro. Conventional techniques, such as benchtop microscopy and fiber photometry, offer high resolution but have notable limitations—they are invasive, lack wireless functionality, and are typically restricted to specific regions, making them unsuitable for broader applications requiring bio-implants [1, 2]. In this paper, we propose a novel optical SoC designed to overcome these challenges by enabling non-invasive wireless fluorescence monitoring. This optical SoC eliminates the need for large external hardware, providing mobility, flexibility, and high sensitivity for fluorescence-based sensing at the cellular level.

Existing CMOS-based optical sensors face challenges in implantable use. For instance, the sensor in [3] achieves 50 fA sensitivity but consumes 66 mW and lacks wireless data readout, while the system in [4] offers 2.46 pA sensitivity but requires bulky external hardware for communication and power. Although the ingestible sensor in [5] includes wireless functionality, its size (1.2 × 2.5 cm²) is too large for implantation. Similarly, the smart contact lens controller in [6] supports wireless glucose measurement but lacks the sensitivity for fluorescence sensing. These limitations underscore the need for a compact, integrated optical sensing solution.

This paper proposes the circuit and system design of the optical SoC with 0.5 pA sensitivity, 1 µW average power at size of 2×2.7 mm², shown in Fig. 1. The SoC comprises a configurable optical front-end, LED driver, wireless communication, energy harvesting, and battery management. In addition, it features an integrated photodiode (PD) to detect fluorescence emitted in response to excitation from an external micro-LED [7]. Power for both the SoC and the micro-LED is supplied by a solid-state battery [8], supported by a boosting capacitor. Upon completion of fabrication, the SoC will employ a PCB antenna [9] for wireless power and data transmission, enabling fully autonomous operation, all integrated in a mm-sized implant.

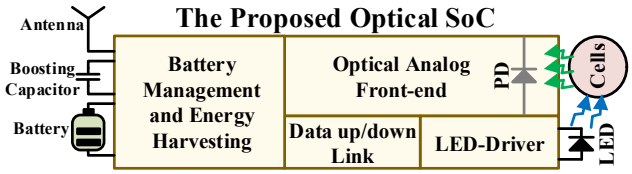

Fig. 1. System view of the proposed optical SoC

One major challenge in implantable optical sensors is the limited power budget, mainly due to the high current needs of the micro-LED. To address this, the proposed design uses a pulsed power management strategy with a fast-settling optical front-end to minimize LED emission and measurement time supported by dual-mode LDOs for efficient power management.

The proposed optical front-end uses a pseudo-resistive (PR) TIA with variable feedback gain, providing high sensitivity while minimizing the power. The front-end achieves 0.5 pA fluorescence current detection through a fast-settling mechanism that stabilizes the TIA during startup, allowing rapid transition to measurement mode. Additionally, dual-mode LDOs in the power management unit enable efficient power gating by providing high current during active phase and ultra-low quiescent current during idle phase. The system supports wireless configurability for both TIA's gain and LED driver's current, allowing optimal adjustment of sensitivity (0.5 pA- 2 pA) and dynamic range (1 nA up to 5 nA). The battery management unit, reported as a previous work of this project [10], incorporates four monitoring units for battery health only consuming 480 pW, enabling continuous operation with minimal user intervention.

The proposed optical SoC offers a comprehensive solution to challenges in implantable optical sensing for cellular monitoring, providing high integration, low power consumption, and wireless communication. This paper is organized as follows: Section II details the system architecture, Section III presents post-layout simulation results and a comparison table, and Section IV concludes the findings.

II. System Description

This section presents the architecture and operation of the proposed optical SoC, which is composed of three main blocks: the Optical Front-end, Wireless Data Uplink/Downlink, Battery Management Unit and Energy Harvester, as depicted in Fig. 2a.

A. Timing and State Diagram of the SoC

The proposed optical SoC operates based on the state machine diagram shown in Fig. 2b. These modes, wirelessly initiated by the user, are designed to minimize power consumption using power gating based on the timing diagram depicted in Fig. 2c.

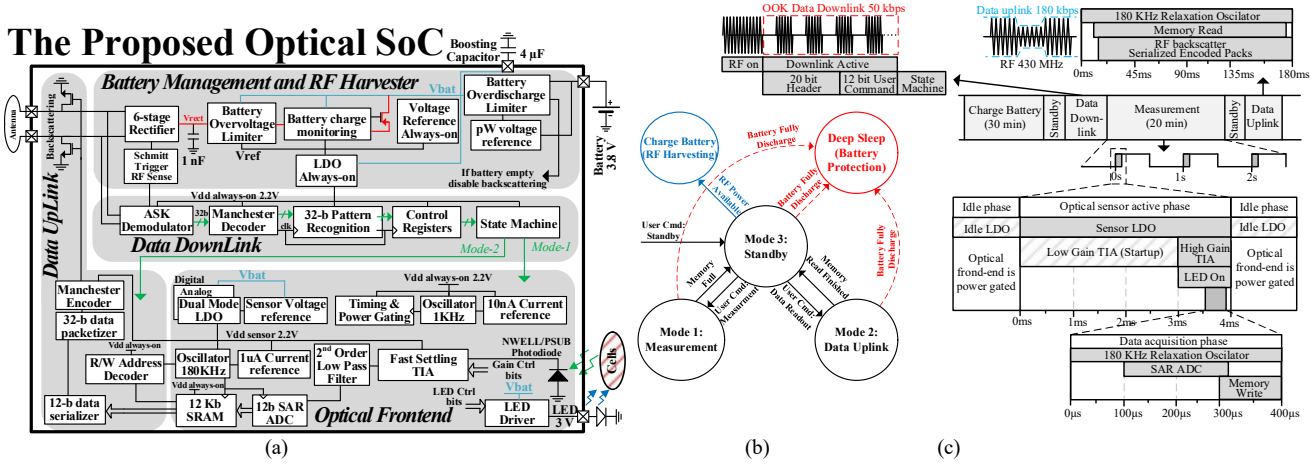

Fig. 2. The operation principle of the proposed optical SoC: (a) The block diagram (b) The state machine (c) The timing diagram

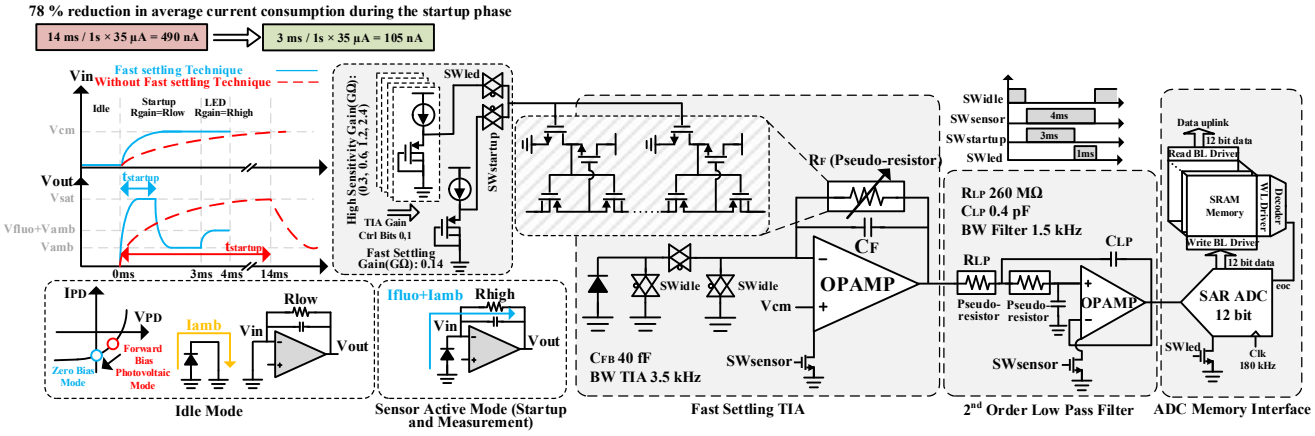

Fig. 3. The implementation of the proposed fast-settling optical front-end and its operation diagram

Measurement mode (Mode 1) is activated by the user command through the wireless downlink. In this mode, the optical front-end is powered to capture and record the reflected fluorescent light from the cells. To conserve power, the micro-LED is only active for a short measurement window of 1 ms while the rest of the front-end is active for 4ms for startup and settling of the TIA operation point before turning on the LED. This brief activation is followed by an idle period of 1023 ms timed by the 1kHz relaxation oscillator and a 10-bit counter. This cycle repeats for 1024 seconds, during which a full fluorescence measurement is captured, digitized, and stored in an on-chip SRAM memory. After memory is full, standby mode automatically starts. Once a full 1024 second fluorescent measurement is finished, data readout mode (Mode 2) is triggered by the user command to encode, pack, and wirelessly backscatter the stored fluorescence data from the memory to a base station for analysis. After a full memory read operation, the standby mode automatically starts. Standby mode (Mode 3) is the default mode of the sensor at which the system minimizes power consumption by deactivating most components. While always-on units, such as the battery management unit monitors the sensor's battery voltage, the state machine keeps the system state and memory holds the measurement data all powered by an always-on LDO. Furthermore, under all the modes if battery voltage drops below deep-discharge-threshold the battery management unit puts the SoC to deep-sleep mode to prevent battery damage.

B. The Proposed Low Power High Sensitivity Optical Front-end

To minimize the average power consumption of the optical front-end during measurement mode, we propose a fast-settling, high-sensitivity PR TIA, as illustrated in Fig. 3. During the 1 ms measurement window, blue light from the LED is emitted onto the cells, and the reflected fluorescence is captured by the 300 µm × 300 µm NWELL/PSUB PD, converting the light into current. This current, in range of picoampere, is then transformed into an output voltage by the PR TIA, which utilizes a low power operational amplifier and a 16-segment linearized PR ladder. The PR ladder provides variable gains of 0.3, 0.6, 1.2, and 2.4 GΩ, wirelessly controlled by a configurable beta multiplier current reference, allowing for adjustable sensitivity and dynamic range.

Before the LED activation, the TIA and current reference must be powered on to be settled considering their slow startup time, which is influenced by ambient light levels, high PR resistance and high PD capacitance (15 pF). This startup time is determined by the slow time constant at the input node (Vin, the negative input node common mode voltage) of the TIA in high-gain configurations, ranging from 10 to 20 ms. To shorten this time, the proposed TIA uses a low-value PR (140 MΩ) feedback loop during the startup period, reducing the time constant and enabling the system to approach the desired operating point more quickly (less than 3ms). Once stabilized, the system switches to high-gain mode for sensitive fluorescence measurements. The transition from low gain to high happens without breaking the feedback loop only by adjusting the bias of PR. By dynamically adjusting the

feedback gain, the design balances fast response time during startup with high sensitivity during measurements, optimizing both power efficiency and measurement accuracy.

Additionally, when the TIA is powered down during the idle phase, the PD can enter forward bias photovoltaic mode due to ambient light, causing the input node to drop below -300 mV, extending startup time or damaging the CMOS. To prevent this, the proposed design includes three switches that shift the PD to a zero-bias region and ground the TIA input, allowing the input voltage to start from zero (contrary to a negative value), enabling a faster startup. The proposed optical front-end includes a 2nd-order low-pass filter (LPF), implemented with PRs to save silicon area, followed by a 12-bit, 12 kS/s SAR ADC, and a 12 kbit 10T low power SRAM.

To power the optical front-end, a dual-mode LDO is proposed, minimizing the power consumption. In conventional designs, when the high-power LDO is off, EA cannot provide bias feedback for power PMOS and loads are disconnected from the ground, during idle mode LDO output voltage drifts to the battery voltage (3.8V), risking damage to the 2.5 V CMOS transistors. To prevent this, the high-power LDO would normally need to stay powered on even during idle periods, resulting in significant power consumption. To overcome this, the proposed design depicted in Fig. 4 switches to a nanowatt error amplifier (EA) during idle mode, reducing power consumption to nanowatt range while maintaining LDO output voltage at 2.2 V, thus ensuring safe operation without compromising efficiency and reusing only one large power transistor. The high-power LDO operates at micro-watt level, activating solely during active measurement periods to optimize overall power consumption. In the idle LDO design, considering that nanowatt power consumption needs extra-large (tens of MΩ) feedback resistors, the idle EA utilizes active PRs, which results in a substantial area reduction. The use of native MOS devices at the input stage of the EAs effectively accommodates usage of a low power two-transistor 313-mV reference voltage in the sensor based on the two-transistor voltage reference introduced in [10]. To ensure low noise analog measurements, the proposed front-end uses separate LDOs for digital and analog circuitry.

C. *The Wireless Data Uplink/Downlink Solution*

To control the sensor's modes and configure the optical front-end gain, and LED current level, a downlink unit with an ASK demodulator (430 MHz RF, 50 kHz data) is used, followed by a Manchester decoder and pattern recognition circuit (Fig. 2a).

The 32-bit data packet includes a 20-bit header, 2 bits for mode selection, 2 bits for gain control, and 2 bits for LED current regulation, supporting four optical power levels. To save power, the downlink unit is power gated via NMOS switches, activated only when a high RF power is detected by the Schmitt trigger in the energy harvester unit. The uplink unit, also power-gated, reads 12-bit data from memory at 180 kHz, serializes it, Manchester-encodes, and packs it into 32-bit packets. During readout, the backscattered bit patterns can unintentionally generate matches with the downlink unit's header due to shared RF signal modulation. To minimize these errors, the headers for the uplink and downlink packets are designed as complementary bit patterns of each other, reducing the false matches and improving reliability. A 20-bit header, much longer than the 12-bit data, enhances error resilience.

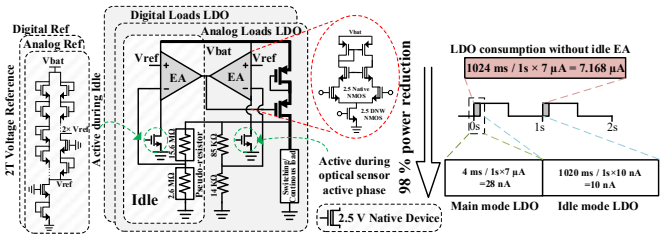

Fig. 4. The implementation of the dual-mode LDO

This length difference reduces the misinterpretation, ensuring reliable packet recognition even in the presence of bit errors

D. *The Battery Management Unit and RF Energy Harvester Solution*

To power the micro-LED's pulsed operation (0.5-2 mA for 1 ms), a 4 µF boosting capacitor and a solid-state thin-film battery with a 5 µAh capacity at 3.8 V from CYMBET are used [8]. A 6-stage cross-connected differential RF rectifier and a 1 nF smoothing capacitor harvest RF energy to recharge the battery from the external RF source. The charging process is regulated to maintain a safe charge voltage range of 4-4.2 V. A four-function 480 pW battery supervisor manages this by connecting the battery to the rectifier only under safe conditions [10]. It also monitors battery discharge voltage, disconnecting all blocks at 3V. It also disconnects the battery charge blocks at 2V, placing the integrated SoC and battery in deep-sleep until recharged again to prevent battery damage.

III. Simulation Results

The proposed optical SoC is designed using 65 nm TSMC low-power technology and has been sent for fabrication. It utilizes 2.5 V thick-oxide transistors for the main design and 5 V drain-extended transistors for the battery/LED/LDO circuit blocks. The chip layout, as shown in Fig. 5, includes various CMOS circuits, PD, LED pads, integration pads, and testing pads, all within a 2 mm × 2.7 mm area. Since the SoC operates on a 3.8 V battery, custom power clamps and ESD circuits are added to protect the I/O pads. To assess the sensor's performance, post-layout simulations at 37°C are done to mimic living body conditions. The results, shown in Fig. 6, compare the dual-mode LDO output voltage and quiescent current (IQ) with and without an idle LDO, demonstrating a drift in output voltage toward Vbat without idle EA. To prevent a disconnect in feedback loop, in the timing of the LDO, first the loads are disconnected and with a small overlap the switch to low I_Q happens. The proposed LDO consumes 7 µA in active mode and 10 nA in idle mode. Fig. 7 illustrates the transient response of the fast-settling optical front-end, indicating the reduced TIA start-up time under 400 pA ambient and 400 pA fluorescent light using fast-settling feedback. The 2.4 GΩ TIA gain results in least input-referred current noise while being slower with less DR and 0.3-0.6 GΩ gains are faster cases with most input-referred current noise and more DR, the default case is 1.2 GΩ. The transimpedance gain and input-referred current noise of the front-end across temperature and process variations before and after the 2nd order LPF are shown in Fig. 8 for 1.2 GΩ TIA gain. The integrated input-referred current noise is 2.3 pA before the LPF and 0.5 pA after, resulting in high sensitivity.

Figure 9 provides a breakdown of the power consumption of the most energy-consuming SoC blocks, compared to LED

power consumption. Given the SoC's on-time of 1024 seconds, the SoC low power usage results only in a 6% usage of the 5 µAh battery capacity, allowing for multiple measurements per charge. In different usage scenarios, such as higher LED light levels, battery consumption can rise up to 10% of the total capacity. Lastly, Fig. 10 presents 1000 Monte Carlo simulation results over process and corner variation for the analog front-end voltage reference, showing a standard deviation of 13.8 mV, which leads to a 3σ variation of 42 mV on the reference and a range of 1.95 V to 2.5 V in front-end's LDO outputs, remaining within the safe operating range of the 2.5 V CMOS devices.

A comparison of the SoC performance and characteristics is made in Table I with other compact optical sensors reported in the literature. Compared to other works, the proposed design offers an implantable form factor that allows for precise in-vivo monitoring. Additionally, the system features wireless data transmission and RF energy harvesting, enabling continuous operation without the need for external hardware or frequent battery replacements. This is a notable advantage over works like [3], which rely on wired data transfer, or [4], which requires larger head-mountable hardware. The proposed SoC also provides a high sensitivity (500 fA) and low power consumption (1 µW), making it more suitable for long-term, implantable monitoring compared to higher power-consuming systems such as [5] (196 µW). These features collectively make the proposed design an ideal solution for biomedical applications requiring implantable, wireless, and energy-efficient systems.

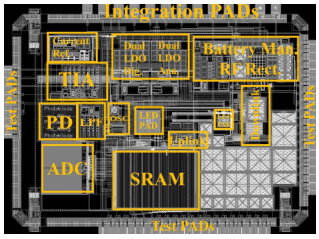

Fig. 5. The chip layout of the SoC in 65 nm TSMC

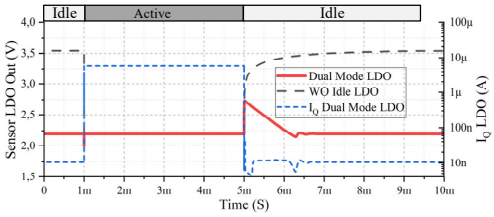

Fig. 6. The transient response of the proposed dual mode LDO

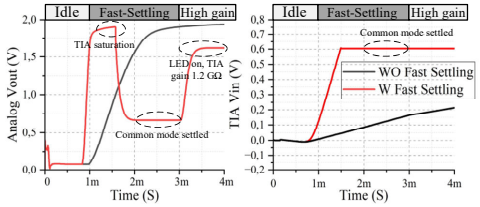

Fig. 7. The transient response of the proposed fast-settling optical front-end

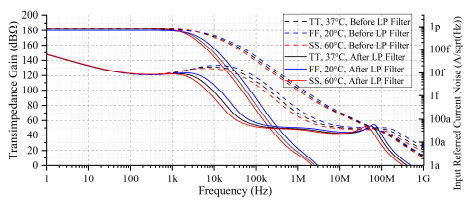

Fig. 8. The transimpedance gain and input referred current noise of the TIA and LPF across temprature variation and differenct process corners

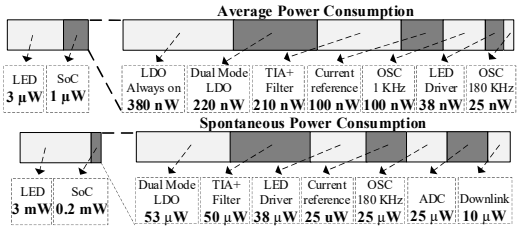

Fig. 9. The average and spontanous power consumptin breakdown of the SoC

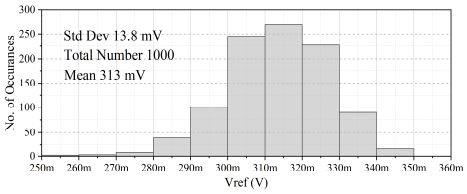

Fig. 10. The 1000 Monte Carlo simulation results over process and corner variation for analog front-end voltage reference

TABLE I. COMPARISON TABLE OF THE PROPOSED OPTICAL SOC WITH SIMILAR WORKS

	This Work	[3]	[4]	[5]	[6]
Optical Conversion Type	PR TIA W ADC	CTIA[c] W ADC	ΣΔ modulator	CTIA	Potentiostat
Power Source	Battery / RF	Wired	Battery	Battery	Battery / RF
Integration	Implantable	Non-implantable	Head mountable	Ingestible pill	Contact lens
Process (nm)	65	65	180	65	130
Optical DR(A)	500 f -1[a] n	50 f-2.3 n	2.46 p -60 n	N.A[c]	100 p -3 µ
CMOS V_{DD}(V)	2.2	N. A	1.8	1	1.6-2.4
$P_{Total,average}$(W)	1 µ	66 m	41 µ	196 µ	143 n
$I_{n,rms}$(A)	500 f	50 f	2.46 p	N.A[d]	100 p

a. For TIA gain 1.2 GΩ
b. Capacitive TIA
c. Reported as: 77 dB below excitation

IV. CONCLUSION

This paper proposes a low-power, optical SoC enabling wireless fluorescence detection. The system integrates a high-sensitivity (500 fA) fast-settling optical front-end, a battery management unit, and wireless data/power transfer, all within a compact form factor consuming only 1 µW average power. The proposed fast-settling transimpedance amplifier and dual-mode low dropout regulators enable rapid startup and minimize the power consumption solving the trade-off between power consumption and sensitivity. The proposed SoC provides a robust solution for non-invasive cellular monitoring, offering significant advancements in implantable biomedical devices.

ACKNOWLEDGMENT

This work is financially supported by the Swedish Foundation for Strategic Research (SSF) under project nr. RMX18-0066. The authors would like to thank the project partners and their team members for close collaboration and valuable discussions, including Prof. Per-Olof Berggren and Dr. Martin Köhler from Karolinska Institutet, Prof. Göran Stemme, Associate Prof. Anna Herland, Associate Prof. Niclas Roxhed, and Prof. Wouter Metsola van der Wijngaart from KTH Royal Institute of Technology.

REFERENCES

[1] S. R. Qasemi, M. Rafati and A. Alvandpour, "A Low Power Front-end for Biomedical Fluorescence Sensing Applications," 2020 IEEE Nordic Circuits and Systems Conference (NorCAS), 2020, pp. 1-6, doi: 10.1109/NorCAS51424.2020.9264996.

[2] M. Rafati, S. R. Qasemi, and A. Alvandpour, "A configurable fluorescence sensing front-end for ultra-low power and high sensitivity applications," Analog Integrated Circuits and Signal Processing, vol. 110, no. 1, pp. 3–17, 2021, doi: 10.1007/s10470-021-01953-5.

[3] L. Hong, H. Li, H. Yang and K. Sengupta, "Fully Integrated Fluorescence Biosensors On-Chip Employing Multi-Functional Nanoplasmonic Optical Structures in CMOS," in IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2388-2406, Sept. 2017, doi: 10.1109/JSSC.2017.2712612.

[4] M. N. Khiarak et al., "A Wireless Optoelectronic Neuroscience Platform for Chronic Fluorescence Sensing in Freely Behaving Rodents," 2018 40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), Honolulu, HI, USA, 2018, pp. 1608-1611, doi: 10.1109/EMBC.2018.8512653.

[5] C. Zhu, L. Hong, H. Yang and K. Sengupta, "Ingestible Bioelectronics: A Packaged, Bio-Molecular, Fluorescence-Based Sensor Array with Ultra-Low-Power Wireless Interface," 2019 IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA, 2019, pp. 212-215, doi: 10.1109/MWSYM.2019.8700834

[6] C. Jeon et al., "A Smart Contact Lens Controller IC Supporting Dual-Mode Telemetry With Wireless-Powered Backscattering LSK and EM-Radiated RF Transmission Using a Single-Loop Antenna," in IEEE Journal of Solid-State Circuits, vol. 55, no. 4, pp. 856-867, April 2020, doi: 10.1109/JSSC.2019.2959493.

[7] Cree, Inc., "Cree® UltraThin® Gen 3 LEDs Data Sheet," 2019. Available: www.cree.com/chips.

[8] Rechargeable Solid State Energy Storage: 5 μAh, 3.8 V, EnerChip CBC005 Datasheet, Cymbet Corp., Elk River, MN, USA, 2012.

[9] N. Terawatsakul, A. Saberkari and A. Alvandpour, "Extending Wireless Power Transfer Range for Self-Powered Micro Devices with mm-size Antenna," 2023 21st IEEE Interregional NEWCAS Conference (NEWCAS), Edinburgh, United Kingdom, 2023, pp. 1-5, doi: 10.1109/NEWCAS57931.2023.10198096.

[10] S. R. Qasemi, M. Rafati and A. Alvandpour, "A Low-Power Battery Charge and Discharge Protection Circuit for Bio-Implantable Sensors in 65nm CMOS," 2024 31st International Conference on Mixed Design of Integrated Circuits and System (MIXDES), Gdansk, Poland, 2024, pp. 68-74, doi: 10.23919/MIXDES62605.2024.10614007.