An OTA with Series-Cascode-Miller Compensation and Anti-Pole-Splitting for a 360-MHz BW Low-Distortion TIA in Sub-6G Broadband RF Receivers

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***Abstract*—This paper presents a fully differential 2-stage operational transconductance amplifier (OTA) for a baseband transimpedance amplifier (TIA) with 360-MHz bandwidth (BW) aiming for applications in Sub-6G broadband direct-conversion receivers. The proposed OTA with folded-cascode input stage incorporates three techniques, including series-cascode-Miller compensation (SCMC), anti-pole-splitting path, and common-mode feedforward (CMFF) to ensure wideband and low distortion of the TIA with shunt feedback. The OTA's BW is extended because the SCMC introduces a zero that cancels the non-dominant pole at the folding node of the OTA, while the anti-pole-splitting path generates a negative capacitance that neutralizes the parasitic capacitance. In addition, the CMFF circuit improves the OTA's common-mode rejection ratio (CMRR) by about 20 dB. Designed in 28-nm CMOS with a 0.12-mm^2 layout area and 16.6-mW power consumption, the TIA demonstrates an SFDR of 103 dB for a 75-MHz, 250-mVpp output, an input-referred noise (IRN) of 85 μVrms, an in-band third-order input intercept point (IIP3) of 37.9 dBm, and an intermodulation-free dynamic range (IMFDR3) of 91.6 dB.**

Keywords—two-stage operational amplifier, compensation, common mode feedforward, transimpedance amplifier, linearity

I. Introduction

Various wireless communication standards operating in the sub-6 GHz bands have continuously evolved to meet the increasing demands for higher data rates and lower latency across emerging applications [1]. Among reported RF receiver topologies, current-mode receivers have gained widespread adoption due to their capability to achieve wide bandwidth and flexibility in channel selection[2]. The transimpedance amplifier (TIA), as the first baseband block in current-mode receivers, determines the upper limits of bandwidth, noise, and linearity of the receiving signal chain, while also providing anti-aliasing filtering for the ADCs[3]. Facing the hard trade-offs between bandwidth, linearity, noise, and etc., it is challenging to design a broadband TIA in advanced CMOS process with low supply voltage.

As is known, the performance of a CMOS TIA is mainly determined by the operational transconductance amplifier (OTA) in it. To achieve high BW, advanced CMOS process is usually indispensable to implement the OTA. However, devices with low intrinsic gain and limited supply voltage impose stringent challenges for the OTA to achieve high gain, broad bandwidth, and wide output swing. Compared to stacked structures, cascaded structures with 2 stages are more preferred under low supply voltage. However, to ensure stability, various compensation techniques are necessary in the OTA design, which may limit the achievable BW. As shown in Fig. 1(a), the classic Miller compensation (MC)[4] inserts a feedback capacitor (C_{MC}) in series with a resistor (R_{MC}) between the input and output stages to split the 2 low-frequency poles and ensure the required phase margin. Ahuja compensation (also known as cascode compensation on a signal path, CCSP)[5] is another widely adopted scheme which feeds the signal back via the cascode transistor M2, thereby eliminating the feedforward path and avoiding the right-half-plane (RHP) zero introduced by feedforward. In addition, cascode compensation on a non-signal path (CCNSP)[6] is a variant of CCSP that slightly extends the bandwidth by reducing the load capacitance on the signal path. Moreover, a variety of hybrid methods have been proposed to optimize the settling time by combining the aforementioned techniques[7,8]. However, it is still difficult to realize a broadband TIA (BW>300MHz) with acceptable power efficiency using the existing compensation techniques.

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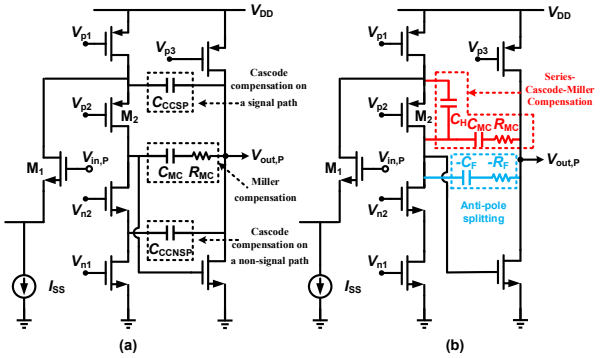

Fig. 1. Compensation methods for 2-stage OTAs: (a) various conventional schemes; (b) conceptual structure of proposed scheme.

This paper proposes a fully differential 2-stage OTA with series-cascode-Miller compensation (SCMC) and anti-pole splitting to extend the OTA's BW. The SCMC introduces a zero which cancels the non-dominant pole at the folding node of the OTA, while the anti-pole-splitting path realizes a negative capacitance which neutralizes the parasitic capacitance. In addition, the OTA adopts a common-mode feedforward (CMFF) technique to improve the CMRR. Based on the proposed OTA, a TIA with 360-MHz BW and 103-dB SFDR is realized in 28-nm CMOS, consuming 16.6mW from a 1.3-V power supply.

II. Proposed OTA Structure and Analysis

The conceptual structure of the proposed compensation scheme is given in Fig. 1(b), while the detailed OTA circuit is shown in Fig. 2(a), with its CMFF and CMFB circuits given in Fig. 2(b). The structure of the TIA with adjustable shunt feedback is given in Fig. 2(c). The mixer preceded the TIA is modeled as a 250-ohm resistor, while the series RC load is used to model the input structure of the followed continuous-time sigma-delta ADC.

A. Series-Cascode-Miller Compensation's Effect

When the anti-pole splitting paths (C_F and R_F) in Fig. 2(a) are not taken into account, the small-signal circuit can be

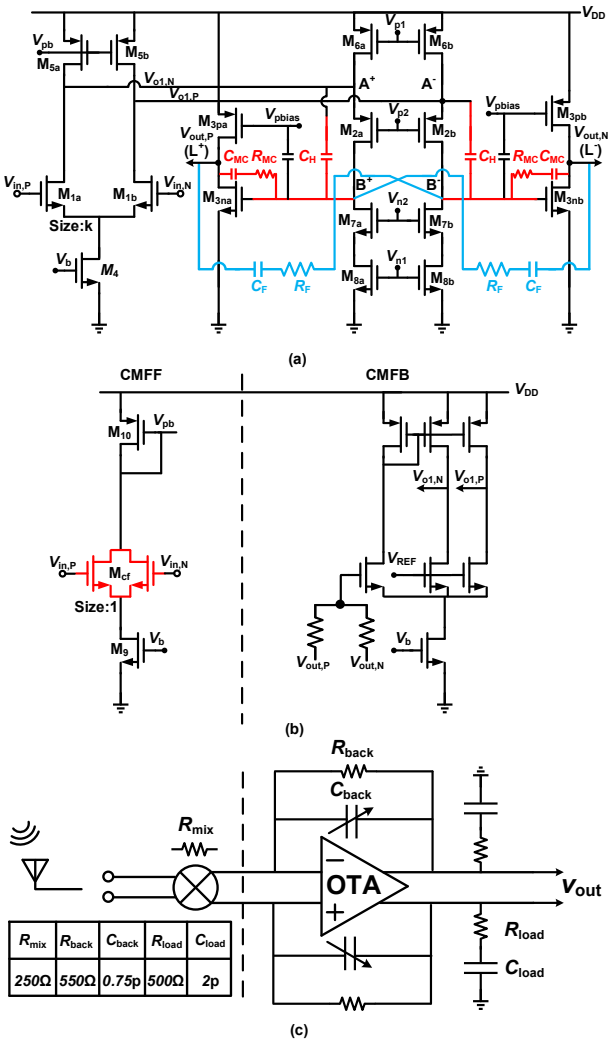

Fig. 2. Circuit structure: (a) proposed 2-stage OTA; (b) CMFF and CMFB circuit of the OTA; (c) TIA structure and circuit parameters.

modeled as shown in Fig. 3(a). To obtain more instructive expressions, the nulling resistors (R_{MC}) are ignored in this model, because they only affect the zero position. The resistance and lumped parasitic capacitance to AC ground at node X are represented by R_X and C_X, respectively (X can be A, B, or L). From Fig. 3, we can obtain following equations:

$$g_{m1}v_{IN} + (g_{m2} + R_A^{-1} + s(C_A + C_H))v_A - sC_Hv_B = 0$$
$$(s(C_B + C_H + C_{MC}) + R_B^{-1})v_B - (g_{m2} + sC_H)v_A - sC_{MC}v_L = 0 \quad (1)$$
$$(g_{m3} - sC_{MC})v_B + (s(C_L + C_{MC}) + R_L^{-1})v_L = 0.$$

Assuming that $g_m \gg R_X^{-1}$ and C_X is much smaller than C_L, C_{MC} and C_H. The OTA's transfer function can be obtained as

$$A_V(s) = \frac{v_L}{v_{IN}} = \frac{g_{m1}(sC_H + g_{m2})(sC_{MC} - g_{m3})}{d_3s^3 + d_2s^2 + d_1s + d_0}$$
$$d_0 \approx g_{m2}R_B^{-1}R_L^{-1}; \quad d_1 \approx g_{m2}g_{m3}C_{MC} \quad (2)$$
$$d_2 \approx g_{m3}C_HC_{MC} + g_{m2}C_LC_{MC}; \quad d_3 \approx C_LC_HC_{MC}$$

As shown, the transfer function contains a RHP zero at g_{m3}/C_{MC}, which can be eliminated by the nulling resistor

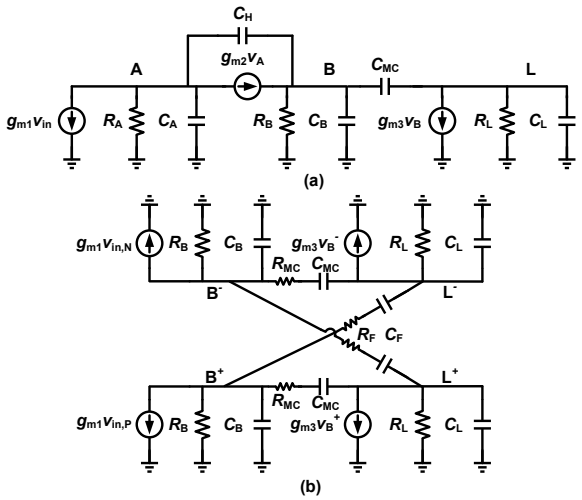

Fig. 3. (a)Small-signal model of the OTA considering only SCMC; (b) Small-signal model of the OTA with anti-pole splitting.

R_{MC}). In addition, an LHP zero at $-g_{m2}/C_H$ is also observed, which is contributed by C_H in the SCMC structure.

Without loss of generality, we assume that the OTA has a dominant pole at

$$\omega_{P1} = -d_0 / d_1 = -1/(g_{m3}R_BR_LC_{MC}). \quad (3)$$

The remaining two nondominant poles of (2) can be found from $d_3s^2 + d_2s + d_1=0$. According to Vieta's formulas, as long as $\Delta = g_{m3}C_HC_{MC} - g_{m2}C_LC_{MC} > 0$ can be guaranteed, the two secondary poles are real poles and can be expressed as

$$\omega_{P2} = -g_{m2}/C_H, \quad \omega_{P3} = -g_{m3}/C_L. \quad (4)$$

As expected, the secondary pole at the folded node can be precisely canceled out by the feedforward zero. As a result, the SCMC scheme ensures that OTA's BW is not limited by the relatively large parasitic capacitance at the folding node.

B. Anti-pole-splitting Using Negative Capacitance

As known, the Miller compensation ensures stability through pole splitting, which drives the dominant pole at the first-stage output node to a much lower frequency while push the secondary pole at the second stage to a much higher frequency. Obviously, Miller compensation usually results in a low BW for the OTA because pole splitting results in a very low-frequency dominant pole.

To further extend the −3-dB bandwidth of the OTA and reduce high-frequency distortion of the TIA, we attempt to introduce an extra feedforward path (R_F and C_F in Fig. 2(a), also termed as ant-pole-splitting path), which can retain the position of the high-frequency pole while increases the dominant pole frequency to a large extent. Unlike that in [9], this design incorporates a nulling resistor in the feedforward path. At low frequencies, the capacitive impedance dominates and the negative capacitance C_F formed by cross-coupling weakens the effect of pole splitting of the Miller compensation, resulting in a dominant pole with higher frequency. At high frequencies, the resistive impedance ensures that the original Miller path remains as the primary feedback path, retaining the position the non-dominant pole generated by pole splitting.

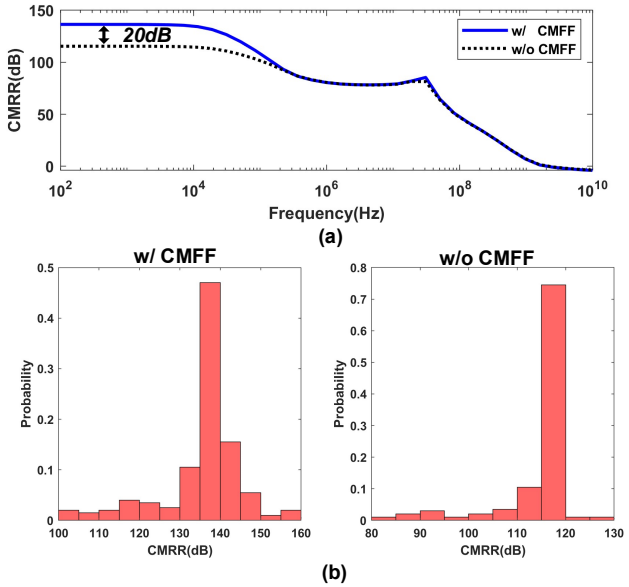

Fig. 4. Simulated CMRR improvement by the CMFF structure: (a) AC simulation; (b) Monte Carlo simulation.

As analyzed in previous subsection, the SCMC realizes cancellation of the pole at the folding node (node A) by adding a LHP zero, thus the small-signal model of the first stage can be simplified. The overall circuit model is illustrated in Fig. 3(b) considering both SCMC and anti-pole splitting path. Similarly, KCL equations can be written for nodes B^+, B^-, L^+, L^-. Considering differential operation, we can obtain:

$$\begin{aligned} g_{m1}v_{IN} + v_B(Z_B^{-1} + Z_F^{-1} + Z_{MC}^{-1}) + v_L(Z_F^{-1} - Z_{MC}^{-1}) = 0 \\ g_{m3}v_B + v_L(Z_L^{-1} + Z_F^{-1} + Z_{MC}^{-1}) + v_B(Z_F^{-1} - Z_{MC}^{-1}) = 0 \end{aligned} \quad (5)$$

where Z_B and Z_F as the differential impedance of the node B and F, respectively, while Z_F and Z_{MC} represent the impedance of the feedforward and Miller compensation paths, respectively.

Assuming that the g_m of all transistors is large enough, the transfer function of the 2-stage OTA can be re-derived as:

$$A_V(s) = \frac{v_L}{v_{IN}} = \frac{g_{m1}(e_2 s^2 + e_1 s + g_{m3})}{h_4 s^4 + h_3 s^3 + h_2 s^2 + h_1 s + h_0}.$$

$$\begin{aligned} &e_2 \approx g_{m3}C_{MC}R_{MC}C_F R_F; \quad e_1 \approx g_{m3}C_{MC}R_{MC} + g_{m3}C_F R_F \\ &h_4 \approx R_{MC}R_F C_F C_{MC} C_B C_L; \; h_3 \approx C_F C_{MC}(R_{MC} + R_F)(C_L + C_B) \\ &h_2 \approx (g_{m3}(R_F - R_{MC}) + 4)C_F C_{MC} \\ &h_1 \approx g_{m3}(C_{MC} - C_F); \quad h_0 \approx R_B^{-1} R_L^{-1} \end{aligned} \quad (6)$$

With the expressions of e_1 and e_2 in (6), the magnitudes of the zeros can be expressed approximately as

$$\omega_{Z1} = -1/(R_{MC}C_{MC}), \quad \omega_{Z2} = -1/(R_F C_F). \quad (7)$$

To ensure stability, the poles need to be located in the left half-plane. Therefore, it is necessary to satisfy that the denominator coefficients $h_i > 0$, that is, C_{MC} is greater than C_F. Without loss of generality, we still assume that the operational amplifier has a dominant pole

$$\omega_{P1} = -h_0/h_1 = -1/\left[g_{m3}R_B R_L (C_{MC} - C_F)\right] \quad (8)$$

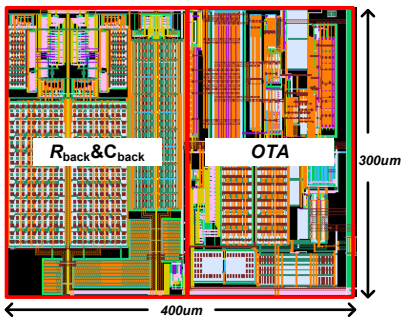

Fig. 5. Layout of TIA

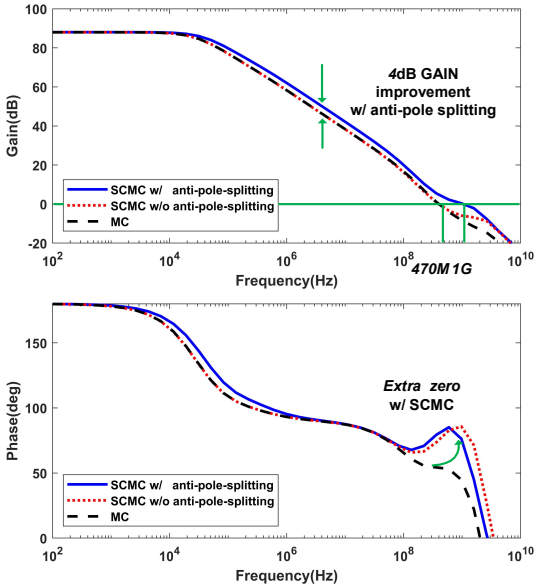

Fig. 6. Frequency response of the TIA's loop transfer function.

The remaining 3 non-dominant poles of (6) are found from $h_4 s^3 + h_3 s^2 + h_2 s^1 + h_1 = 0$. There is no clear order of magnitude relationship among these 3 nondominant poles. However, according to Vieta's formulas, we can obtain

$$\begin{aligned} \omega_{P2} + \omega_{P3} + \omega_{P4} &= -h_3/h_4 \\ &= -1/[(R_{MC} \parallel R_F)(C_L \oplus C_B)], \end{aligned} \quad (9)$$

$$\begin{aligned} \omega_{P2}\omega_{P3}\omega_{P4} &= -h_1/h_4 \\ &= -g_{m3}(C_{MC} - C_F)/(R_{MC}R_F C_L C_B C_{MC} C_F). \end{aligned} \quad (10)$$

The symbol $\oplus$ represents series connection. When there is no anti-pole splitting path, there will be two non-dominant poles with the following relationships

$$\omega_{P2} + \omega_{P3} = -1/[R_{MC}(C_L \oplus C_B)], \quad (11)$$

$$\omega_{P2}\omega_{P3} = -g_{m3}/(R_{MC}C_L C_B). \quad (12)$$

According to (9), in order to ensure that the non-dominant poles are as far away as possible, it is necessary to satisfy $R_F > R_{MC}$, which is in consistent with the intuition. Comparing (10) with (12), the additional pole frequency is at around $(C_{MC}\text{-}C_F)/(R_F C_{MC} C_F)$, which is slightly smaller than the zero ω_{Z2} in (7) (if $C_F > 0.5C_{MC}$), thereby leading to an improvement in phase margin. Therefore, the design guideline after introducing the anti-pole splitting path can be described as: C_F is set to 0.5 C_{MC}, with adjustments made to R_{MC} to ensure that R_F is greater than 3 R_{MC}.

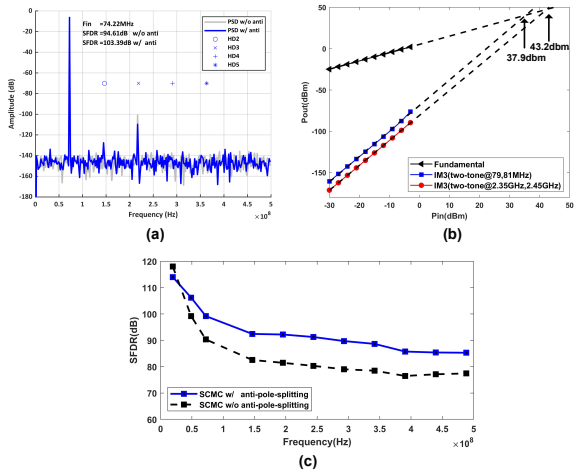

Fig. 7. Linearity simulation of the TIA: (a) single-tone PSD; (b) IIP3 with 2-tone input; (c) SFDR varying with input frequency.

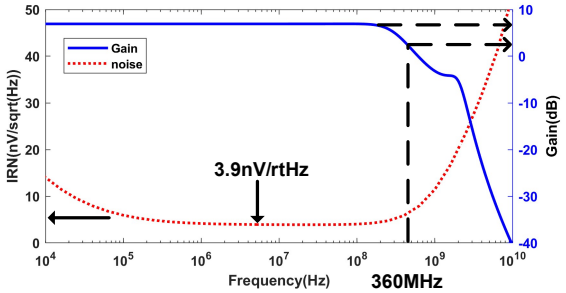

Fig. 8. Simulated Voltage gain and input-referred noise of the TIA.

C. Common Mode Feedforward

Common-mode interference will directly affect the normal operation of the RF receiver and impair its dynamic range, especially in the TIA. Improving the CMRR of the OTA not only enhances the closed-loop CM noise rejection capability of the TIA in small-signal scenarios but also provides a wider stable input range for large signals [10].

As shown in Fig. 2(b), besides the CMFB circuit, this design also inserts a CMFF circuit to compensate the limited impedance of the tail current source (M4) for the input pair of the OTA. As shown, an auxiliary input pair (with a size of $1/k$ relative to the input pair) senses the variation of the input CM level. Variations in the input CM level is converted into a slight current because of the limited impedance of M9, which is replicated by a current mirror and then injected into the 1st-stage amplifier. As a result, the CM current variation caused by the limited impedance of M4 can be compensated to a large extent. The AC and Monte Carlo simulation in Fig. 4 show that the CMFF structure improves the simulated low-frequency CMRR by about 20dB.

III. Simulation Results of TIA

A TIA with the proposed OTA (as shown in Fig. 2(c)) is designed for a wideband direct-conversion RF receiver in 28-nm CMOS. The layout area of the TIA is 0.12mm^2, as shown in Fig. 5. The design operates under a supply voltage of 1.3 V with a total power consumption of 16.6 mW.

Based on the proposed structure, we conducted simulations to validate its performance, as discussed below.

TABEL I. TIA Performance Summary and Comparison.

Parameter	This work[a]	ISCAS'23 [11][a]	SSCL'22 [12]	JSSC'18 [13]
Technology [nm]	28	40	28	28
Supply [V]	1.3	1.2	1.5	1.8
Power [mw]	16.6	10.4	17.0	5.4
Filter Order(N)	1	1	1	1
ICMR Extend	Yes	Yes	No	No
BW_{-3dB} [MHz]	360	50	500	20
IRN[b] [uV_{RMS}]	2.4	10.1	6	13.1
IB IIP3 [dBm]	37.9	31.6	33	31.5
OB IIP3 [dBm]	43.2	50.6	42	50.5
IMFDR3[c] IB [dB]	91.6	79.0	82.9	77.4
FoM[d] [dB]	195.0	175.8	187.6	173.1

[a.] Simulation results.
[b.] IRN is normalized to 10MHz, assuming thermal noise is dominant.
[c.] IMFDR3 = 2/3(P_{IIP3}- P_{IRN}).
[d.] Fom = IMFDR3IB+10log(N • BW/Power).

The frequency responses of the TIA's loop transfer function are depicted in Fig. 6 for 3 scenarios with the same current consumption. As shown, compared to traditional Miller compensation, the proposed SCMC improves the phase response by adding an extra LHP zero. Furthermore, the introduction of the anti-pole splitting path expands the 3-dB bandwidth without incurring additional power overhead. Simultaneously, within the frequency band of interest, the loop gain is increased by approximately 4dB.

Time-domain simulation with a 75-MHz single-tone 250-mVpp output reveals that the TIA with only SCMC compensation achieves an SFDR of 94dB. With the addition of the anti-pole splitting path, the SFDR increases by approximately 9dB, as shown in Fig. 7(a). The two-tone simulation in Fig. 7(b) shows an in-band (IB) IIP3 of about 37.9dBm. Fig. 7(c) further plots the simulated SFDR varying with input frequency, showing obvious SFDR improvement at high frequencies brought by the proposed scheme. The closed-loop gain and input-referred noise of the entire TIA are given in Fig. 8, showing a voltage gain of 7 dB (considering the 250-Ω resistance of the passive mixer) with a BW of 360 MHz. The input-referred equivalent noise integrated from 1 MHz to 360 MHz is 85.3 μVrms.

The performances of the TIA are summarized in Table I, with comparison to other recent TIA with 1st-order filtering. The TIA in [12] utilizes on-chip inductors and achieves a wider BW. Compared to the structures without inductors in [11] and [13], this design achieves a wider BW. Furthermore, the proposed circuit achieves the best performances regarding to IB noise and the Figure of Merit (FOM). Additionally, this design optimizes the input common-mode range (ICMR) to tolerate common-mode interference.

IV. Conclusion

This paper proposes a 2-stage OTA design method which extends the BW bandwidth and reduces distortion using SCMC combined with anti-pole splitting and CMFF. The SCMC introduces an additional zero through high-frequency paths, thereby extending the bandwidth of the folded-cascode structure. Based on Miller compensation, the anti-pole-splitting path with series RC extents BW through weaking the pole splitting at low frequencies while maintaining the Miller path at high frequencies. Additionally, the CMFF circuit improves the small signal CMRR. The OTA is implemented in a wideband TIA circuit with 28-nm CMOS, achieving 360MHz BW and with 103-dB SFDR, while consuming 16.6mW from a 1.3-V supply voltage.

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