2026 IEEE International Symposium on Circuits and Systems (ISCAS) | 979-8-3315-7769-8/26/$31.00 ©2026 IEEE | DOI: 10.1109/ISCAS66217.2026.11562825

A 0.74 pJ/bit 10 Gbps PAM-4 Transceiver with Triple TIA Termination and Power-saving Addition-only Driving for Parallel Memory Interface Channels

[1]Junsen He, [1]Kiho Seong, [1,2]Donghyun Yoon, [3]Seung-Myeong Yu, [3]Junyoung Song, [2]Youngdon Choi, [2]Jung-Hwang Choi, and [1]Tony Tae-Hyoung Kim

[1]Nanyang Technological University, Singapore, [2]Samsung Electronics, Hwaseong, Korea, [3]Incheon National University, Incheon 22012, South Korea

***Abstract*—This paper presents a 10Gbps 0.74pJ/bit PAM-4 transceiver using a triple transimpedance amplifier (TIA) termination receiver with a power-saving addition-only driving. The proposed addition-only main driver removes the large static current for the intermediate-level generation and reduces the total transmitter power by 36.33%. This work also utilizes an addition-only feed-forward equalizer (A-FFE) for further power reduction. In the receiver, a triple TIA with symmetric threshold voltages is proposed to enhance the eye height by separating the three eyes. The total eye height is improved by a factor of 6.53. Moreover, a RZ (return-to-zero) decoder is employed to remove the RZ-to-NRZ (non-return-to-zero) converters for power-saving. The proposed transceiver was fabricated in a 65 nm CMOS process and achieves an energy efficiency of 0.74pJ/bit at 10 Gbps.**

***Keywords*—Parallel interconnection, memory interface, PAM-4 transceiver, power saving, eye enhancement.**

I. Introduction

The increasing need for high bandwidth and parallel interconnections in memory interfaces continues to rise. Fig. 1 shows three structures for the memory interface. Non-return-to-zero (NRZ) signaling features a simple structure but encounters significant channel loss and high power consumption. NRZ is a widely used signaling method in digital communication, where binary data is transmitted as two distinct voltage levels.

Pulse Amplitude Modulation with Four Levels (PAM-4) can transmit one more bit in one unit interval (UI). Therefore, PAM-4 requires a lower clock frequency but brings two significant challenges. First, the smaller voltage level differences between adjacent levels make PAM-4 more susceptible to noise and cause signal distortion. Second, the two intermediate voltage levels (10 and 01) generate large static current in conventional main driver and consume large static power. In conventional analog-type PAM-4 drivers, intermediate level generation requires the simultaneous activation of both pull-up and pull-down strengths, leading to significant static power consumption [1-4] . Furthermore, conventional feed-forward equalizers (FFEs) employ post taps with reduced driving strengths to equalize transmitter output (TX), but this structure also exhibits considerable static current [1-3]. Even when equalization is not required, the continuous static current in the FFE driver results in unnecessary power dissipation.

Recently, PAM-3 with a dual trans-impedance amplifier (TIA) receiver has been proposed [5] to amplify the receiver input (RX) eye height for a better bit error ratio (BER). However, the dual TIA structure can be only applied to PAM-3. To broaden the application of the TIA receiver structure, a triple TIA design is proposed in this PAM-4 work. The proposed triple TIA structure amplifies the PAM-4 RX to improve eye-opening and BER. Moreover, an addition-only main driver is designed to eliminate the static current when generating the two intermediate voltage levels. Addition-only feed-forward equalizer (A-FFE) [4,6] and non-RZ-to-NRZ design are also implemented for power saving. Finally, for better BER, grey code encoding and decoding are applied in this work.

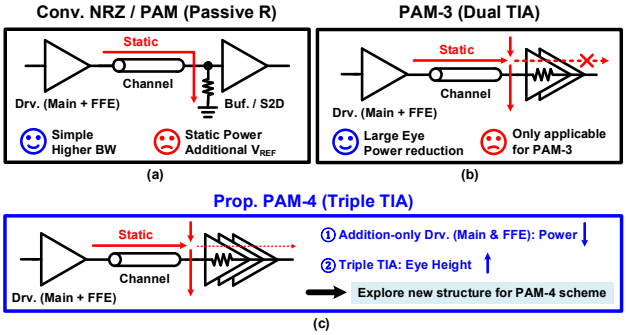

Fig. 1 Three memory interface architectures.

II. Proposed PAM-4 Transmitter

Fig. 2 (a) shows the top block diagram of the proposed PAM-4 transmitter (Tran) for on-chip transmission lines and off-chip bonding wire channels. The pattern generator provides the non-return-to-zero (NRZ) pseudo-random bit stream (PRBS) 7 pattern. The NRZ signal is encoded to a grey code PAM-4 signal. The encoder (main + FFE) generates the control signals to drive the main driver and FFE driver.

For on-chip transmission lines, the main driver and FFE driver operate together to maintain high fidelity in TX, compensating for inter-symbol interference (ISI) and signal degradation. In contrast, for off-chip bonding-wire channels, the FFE is not utilized due to the negligible ISI in the bonding-wire channels.

A. Proposed Main Driver

Fig. 3 compares the conventional main driver with the proposed main driver and the left of Fig. 4 illustrates the detail implementation of the proposed main driver. There are four voltage levels in PAM-4 signaling type: High-High (HH), High-Low (HL), Low-High (LH) and Low-Low (LL). In both design, HH and LL levels generations operate on similar principles where only PMOS(s) drive HH level and only NMOS(s) drive LL level. For the intermediate levels

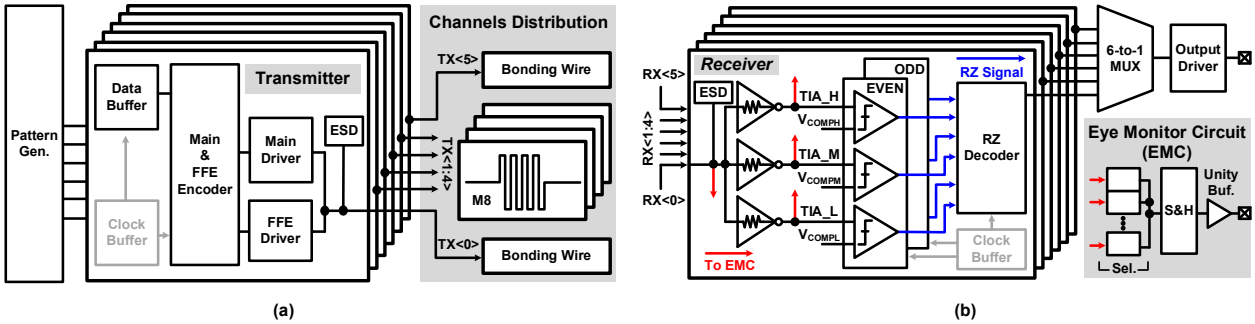

Fig. 2 Block diagram of the proposed (a) transmitter and (b) receiver.

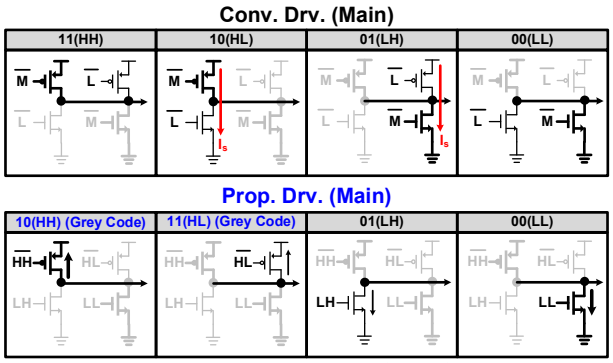

Fig. 3 Operation of the proposed main driver.

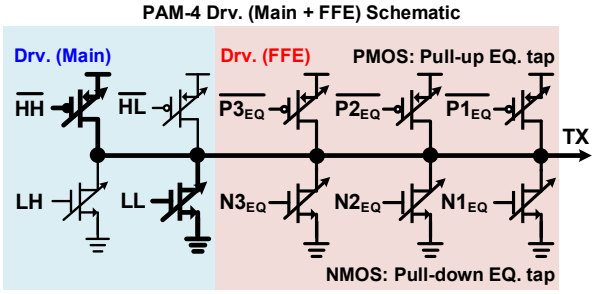

Fig. 4 Driver (main and FFE) schematic.

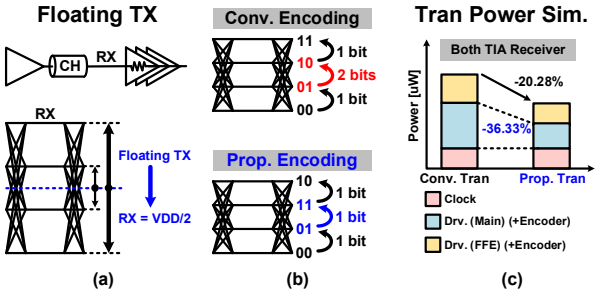

Fig. 5 (a) Floating TX analysis (b) grey code encoding and (c) transmitter power simulation .

comparison, in the conventional design, the PMOS and NMOS are turned on together to generate the two intermediate voltage levels, resulting in significant static current (Is). In the PAM-3 with dual TIA receiver [5], the self-driven receiver (SDR) can generate the Mid-level voltage by itself if TX is floating. Similarly, in the proposed design (PAM-4 with TIA structure), the TIA output also becomes the half supply voltage if TX is floating. Therefore, the two intermediate levels are generated by a small pull-up and a small pull-down strength (Fig. 5 (a)) to eliminate the static current in the main driver for power reduction. In this approach, the HL level can be driven by a weak PMOS transistor (small pull-up strength). Similarly, the LH level is driven by a weak NMOS transistor (small pull-down strength).

Half-rate encoding, typically utilized in DDR interfaces, has also been employed in this work. The 2-to-1 multiplexer (embedded in Main & FFE Encoder) can convert the two 2-UI signals (full-rate signals from even mode and odd mode) into one 1-UI signal (half-rate signal) for PAM-4 signal generation.

B. Addition-only Feed-forward Equalizer for PAM-4

To further reduce the power consumption, an A-FFE has been implemented in this work. In the PAM-4 signal, there are six voltage rising transitions and six voltage falling transitions. Therefore, three identical PMOS transistors and three identical NMOS transistors are designed for TX equalization (the right of Fig. 4). There are only three cases during FFE operation: First, if TX requires pull-up strength, only PMOS(s) in FFE driver are operating; Second, if TX requires pull-down strength, only NMOS(s) in FFE driver are operating; Third, all six transistors are disabled if no equalization requires. Therefore, this FFE encoder design ensures no static current in the FFE driver, thereby reducing power consumption. Moreover, this approach ensures that the control signals are efficiently managed for all voltage level transitions, allowing for individually equalizing the eye diagram [4]. The FFE encoder also incorporates a 2-to-1 multiplexer to convert full-rate signals into half-rate signals.

C. Grey Code Encoding and Power Simulation Results

Moreover, grey code encoding is applied in the Tran design (Fig. 5 (b)). For the conventional encoding, there are two-bit differences between the two intermediate levels. In grey code encoding, only one-bit changes between the two intermediate levels. Therefore, BER can be improved when decoding the two intermediate levels. The proposed main driver reduces power by 36.33% and the total Tran power, including peripheral circuits, by 20.28%, as shown in Fig. 5 (c).

III. Proposed PAM-4 Receiver

Fig. 2 (b) illustrates the overall structure of the proposed receiver. For single-ended PAM-4 signals, achieving better signal integrity and higher data rates is challenging due to the limited eye height. Differential PAM-4 signals, on the

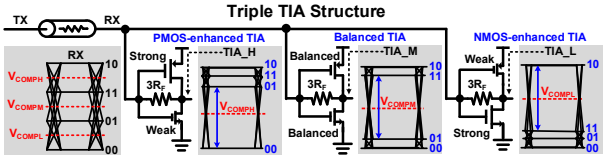

Fig. 6 Triple TIA structure.

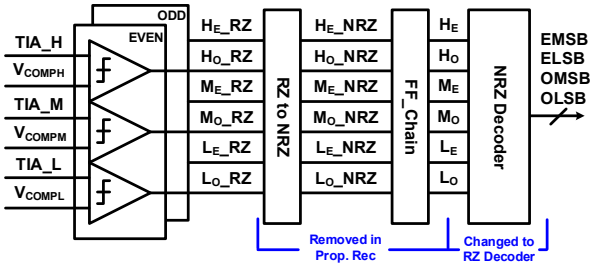

Fig. 7 Operation of NRZ decoding and improvement in RZ decoding.

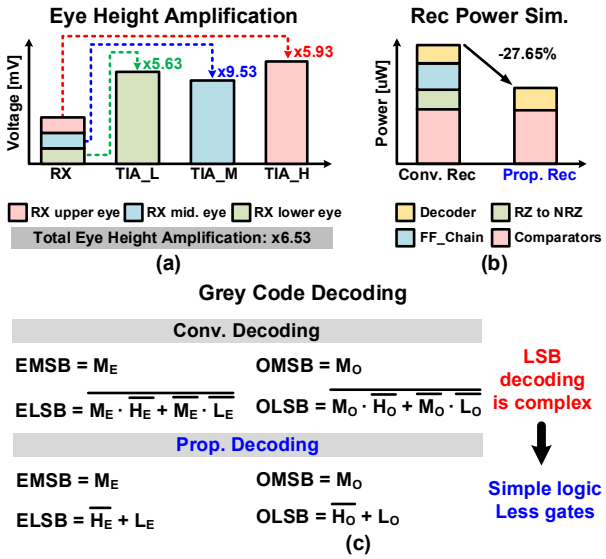

Fig. 8 (a) Eye height amplification analysis (b) receiver power simulation and (c) grey code decoding comparison.

other hand, lead to high power consumption. PAM-3 with single and dual TIA offers improved energy efficiency and better eye height, but it is limited to PAM-3 signalling. To broaden the TIA application, a novel triple TIA structure is proposed in this work. The triple TIA structure independently generates and amplifies the top, middle, and bottom eyes. Additionally, the floating RX self-generates the half supply voltage at TIA output, allowing the usage of small pull-up and pull-down strengths to generate the two intermediate levels, leading to reduced power consumption.

The outputs of the TIA are sensed by slicers which designed by strong-arm NMOS latches. Slicers transfers the TIA outputs to return-to-zero (RZ) signals. These RZ signals are decoded, recovering back to the original four 2UI NRZ signals: A_OUT, B_OUT, C_OUT, and D_OUT. This work removes RZ-to-NRZ converters for saving power but still achieve the same function. Moreover, TIA outputs and RX also operate in the eye monitoring circuit (EMC) for eye measuring. EMC is designed based on sampling & holding the voltage level data and recovered to the appropriate eye diagrams for analysis.

A. Triple TIA Structure for PAM-4

Fig. 6 presents the triple TIA structure for PAM-4, which combines the dual TIA structure [5] and single TIA structure [7]. The signal amplitude of RX is constrained by the supply voltage, limiting the maximum theoretical eye height to 0.33 VDD. To overcome this limitation, the triple TIA structure is proposed which uses three different threshold voltages to enhance the eye height.

The triple TIA includes three TIAs: PMOS-enhanced TIA (PE TIA), NMOS-enhanced TIA (NE TIA), and a Normal TIA. The PE TIA, with a strong PMOS and a weak NMOS, amplifies the top eye of RX. Its threshold voltage, V_{COMPH}, corresponds to the center of the top eye of RX. The NMOS-enhanced TIA (NE TIA), with a strong NMOS and a weak PMOS, amplifies the bottom eye of RX, with its threshold voltage V_{COMPL} is the center of the bottom eye of RX. The Normal TIA amplifies the middle eye of RX, with the threshold voltage V_{COMPM} which corresponds to the center of the middle eye of RX. V_{COMPM} is 0.5VDD while another two threshold voltages, V_{COMPH}, and V_{COMPL}, are symmetrical around 0.5 VDD, maintaining the overall equivalent threshold voltage.

The proposed triple TIA separates the top, middle, and bottom RX eyes and amplifies each eye individually. The PE TIA amplifies the top RX eye. The balanced TIA and NE TIA are similar. The feedback resistance is tripled in the triple TIA compared to dual TIA and single TIA. Fig. 8 (a) illustrates the eye height amplification results. The total eye height can be amplified by a factor of 6.53.

B. Return-to-zero (RZ) Decoding

An conventional NRZ decoding scheme is illustrated in Fig. 7. The comparator is designed by a strong-arm latch, producing an RZ output signal. For easier processing in the subsequent operations, an RZ-to-NRZ converter is implemented. In conventional work [8], a CML-based latch-type converter was proposed, but it consumed significant static current. Another approach utilizes logic gates (inverters, NAND, and BUF gates) for the RZ-to-NRZ conversion, but this design also consumes additional power. To enhance power efficiency, the RZ-to-NRZ converters can be removed. As a result, the decoder not only decodes the RZ signals but also converts to NRZ signals directly, thereby reducing total power consumption. Fig. 8 (b) demonstrates achieving 27.65% reduction in power consumption by removing the converter. Last but not least, compared with conventional decoding, grey code decoding is much simpler for LSB decoding (Fig. 8 (c)). The simpler equations require fewer logic gates, resulting in lower power consumption.

IV. Measurements

The proposed PAM-4 transceiver and on-chip channels are fabricated in a 65 nm CMOS process. Fig. 9 (a) presents the die photo, with the off-chip channels which are designed by bonding wires (Fig. 9 (b)). Fig. 9 (c) shows the on-chip channel schematic and Fig. 9 (d) shows the corresponding characteristics. The on-chip channels in [5] are implemented for testing. The channel length is 6 mm, width is 2 um and pitch is 5 um. The ESD diodes are added to protect the Tran

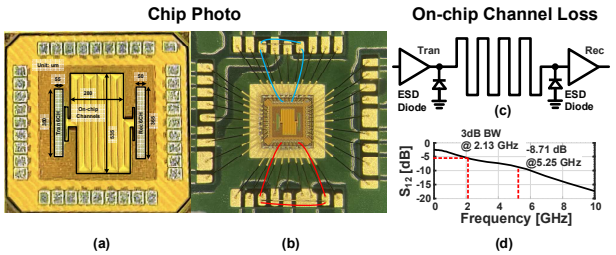

Fig. 9 (a) Chip photo (b) off-chip channel (bonding wires) (c) On-chip channel schematic and (d) corresponding characteristics.

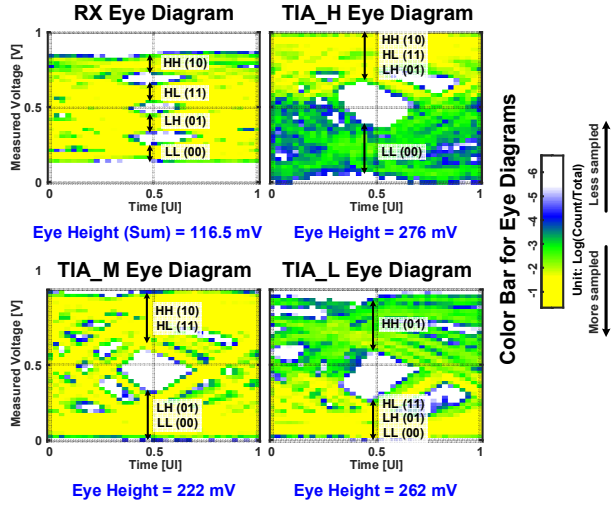

Fig. 10 Measured TIA output eye diagrams.

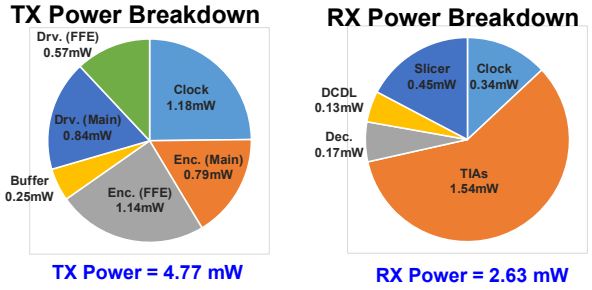

Fig. 11 Power breakdown of TX and RX.

and Rec and emulate high channel loss. The 3 dB bandwidth and channel loss at 5.25 GHz are measured at 2.1 GHz and -8.71 dB, respectively. In Fig. 10, the eye diagram of RX and three TIA outputs are measured at 10 Gbps using EMC in Fig. 2 (b). The RX eye heights (upper, middle, and lower eyes) are 46.6 mV, 23.3 mV, and 46.6 mV, respectively. The PE, balanced and NE TIA output's eye heights are 276 mV, 222 mV, and 262 mV, respectively. Fig. 11 show the transmitter and receiver power breakdown. The total transmitter power is 4.77 mW and the receiver power is 2.63 mW. In the transmitter, the FFE encoder consumes the largest power because of the complex encoding for the six control signals (three for PMOS and three for NMOS). In the receiver, the triple TIA consumes the largest power due to its analog structure

Fig. 12 presents the measured BER bathtub curve of the center channel, which has the largest crosstalk. At 10 Gbps,

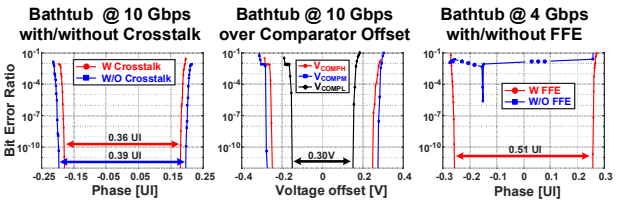

Fig. 12 Bathtub measured results.

TABLE I. PERFORMANCE COMPARISON TABLE

Performance Summary & Comparison Table

	This work	ISSCC23 [1]	VLSI22 [2]	CICC22 [3]	JSSCC21 [4]
Process [nm]	65nm CMOS	4nm FinFET	28nm CMOS	28nm CMOS	65nm CMOS
Modulation	PAM4	PAM4	PAM4	PAM4	PAM4
Termination	Tri-TIA	TX(20Ω)-RX(50Ω)	CTLE With Passive R	External Passive R	External Passive R
Number of Channel	4	4	8	8	1
Data Rate [Gbps]	10Gbps	16Gbps	40Gbps	60Gbps	28Gbps
Energy Efficiency [pJ/b]	0.74	0.764	2.02	1.67 (Only Tran)	0.64 (Only Tran)
Eye Width [UI]	0.36	0.37	0.2 (1E-6)	0.36 (TX)	0.16
Area/Channel [mm^2]	0.00625	0.00726	N.A.	N.A.	0.033
Supply	1	0.75 / 0.6	1.2 / 0.95	1.2	1 / 0.6

the proposed transceiver shows the 0.36 UI with crosstalk. If the other channels are disabled, the eye width increases to 0.39 UI (the left of Fig. 12). The BER over the comparator reference voltage (V_{COMPH}, V_{COMPM}, and V_{COMPL}) offset is shown in the middle of Fig. 12. V_{COMPH}, V_{COMPM}, and V_{COMPL} margins are 495 mV, 545 mV, and 300 mV, respectively. Also, the BERs with and without FFE are compared at 4 Gbps, as shown in the right of Fig. 12. When the FFE is disabled, BER is higher than 10^{-6} for the entire phase. On the other hand, the eye width achieves 0.51UI with FFE enabled. The performances of recent PAM transceivers are compared in Table I. The proposed transceiver achieves the best energy efficiency of 0.74 pJ/bit among the PAM-4 transceivers with a data rate of 10Gbps. The active area of the proposed transceiver per channel is 0.00625 mm^2, which makes it suitable for next-generation memory interface applications.

V. CONCLUSION

In this article, a 10 Gbps PAM-4 Transceiver with four parallel on-chip channels and two off-chip bonding wire channels has been proposed. In high-speed memory interfaces, half-rate structure is commonly implemented to remove the number of full-rate nodes and improve signal integrity. Therefore, encoding and decoding which are based on the half-rate structure are also applied in this work. To reduce the power consumption, addition-only main driver and FFE driver are applied. A novel triple TIA has been designed to separate and amplify RX eye for better bit error ratio. RZ-to-NRZ converters have been removed for power reduction but achieving identical operational functions. At the maximum data rate of 10Gbps, the total power consumption of one transceiver is 7.4 mW and the corresponding power efficiency is 0.74 pJ/bit.

ACKNOWLEDGMENT

This work was supported by Ministry of Education, Singapore, under AcRF Tier-1 (RG136/23).

REFERENCES

[1] J. Jin *et al.*, "A 4nm 16Gb/s/pin Single-Ended PAM4 Parallel Transceiver with Switching-Jitter Compensation and Transmitter Optimization," ISSCC 2023: 1-3.

[2] H. N. Rie *et al.*, "A 40-Gb/s/pin Low-Voltage POD Single-Ended PAM-4 Transceiver with Timing Calibrated Reset-less Slicer and Bidirectional T-Coil for GDDR7 Application," IEEE Symp. VLSI Circuits 2022: 148-149.

[3] J. Kim *et al.*, "A 60-Gb/s/pin single-ended PAM-4 transmitter with timing skew training and low power data encoding in mimicked 10nm class DRAM process," CICC 2022: 1-2.

[4] Y. -U et al., "A 0.64-pJ/Bit 28-Gb/s/Pin High-Linearity Single-Ended PAM-4 Transmitter With an Impedance-Matched Driver and Three-Point ZQ Calibration for Memory Interface," JSSC 2021: 1278-1287.

[5] D. Yoon*, J. He* et al., " A 10.5 Gbps 0.55 pJ/bit PAM-3 Transceiver Using a Self-driven Dual TIA Receiver and Floating Impedance Matching for Parallel On-chip Transmission Lines," A-SSCC 2024: 1-3.

[6] C. Moon *et al.*, "A 20 Gb/s/pin 1.18pJ/b 1149μm^2 Single-Ended Inverter-based 4-tap Addition-Only Feed-Forward Equalization Transmitter with Improved Robustness to Coefficient Errors in 28nm CMOS," *ISSCC 2022*, pp. 450-452.

[7] H. Park *et al.*, "A 0.385-pJ/bit 10-Gb/s TIA-Terminated Di-Code Transceiver with Edge-Delayed Equalization, ECC, and Mismatch Calibration for HBM Interfaces," ISSCC 2022: 1-3.

[8] T. Toifl et al., "A 22-Gb/s PAM-4 receiver in 90-nm CMOS SOI technology," IEEE J. Solid-State Circuits, vol. 41, no. 4, pp. 954–965, Apr. 2006.